Experiment No. 3

Clipping and Clamping Circuits

Object:

To steady the diode applications in a clipping and clamping circuits.

Apparatus:

1. Function Generator.
2. Oscilloscope.
3. DC Power Supply.
4. Breadboard, Diodes, Capacitors and Resistor.

Theory:

This experiment studies the applications of the diode in the clipping & clamping operations.

1. Clipping Circuits:

the Figure (l) shows a biased clipper, for the diode to turn in the input voltage must be greater +V, when V_m is greater than +V , the diode acts like a closed switch (ideally) & the voltage across the output equals +V , this output stays at +V as long as the input voltage exceeds +V.

when the input voltage is less than +V , the diode opens and the circuit acts as a voltage divider, as usual , R_L should be much greater than R, in this way , most of input voltage appears across the output.

The output waveforms of Figure (1) summarize the circuit action. The biased clipper removes all signals above the (+V) level.

2. Clamping Circuits:

A clamper does is adding a DC component to the signal. In Figure (2) the input signal is a sinewave, the clamper pushes the signal upward, so that the negative peaks fall on the 0V level. As can see, the shape of the original signal is preserved, all that happen is a vertical shift of the signal.

We described an output signal for a positive dampen- On the Figure (2) shown

represents a positive clamper ideally here how it is works. On the first negative half cycle of input voltage, the diode turns on.

At the negative peak, the capacitor must charge to V_p with polarity shown. Slightly beyond the negative peak, the diode shunts off**.**

Procedure:

Clipping Circuit:

1. Connect the circuit shown in Figure (3).
2. Ensure that the variable DC is at minimum and the source is at $10V_{P.P}$.
3. Observe and Sketch the input and output waveforms.
4. Increase the variable DC voltage to 4V, and notice to what voltage are the positive

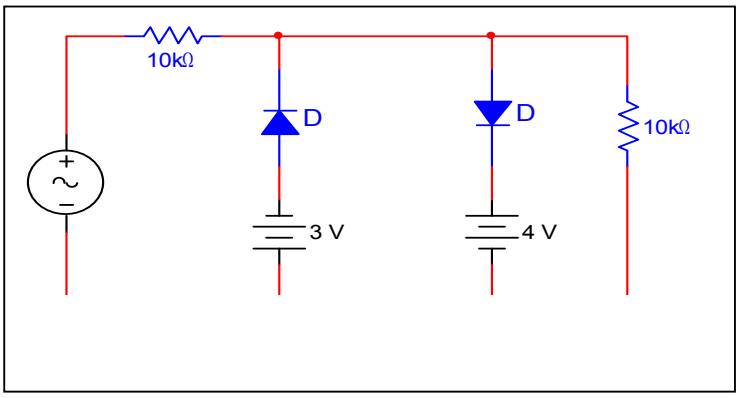
   peaks chopped off, sketch the waveforms.

Clamping Circuit:

1. Connect the circuit shown in Figure (4).
2. Ensure the variable DC is at minimum.
3. Set the sine wave generator frequency to 1KHz and its output amplitude to $10V_{P.P}$.
4. Observe and sketch the input waveform with the variable DC at minimum, Sketch the output waveform.

Discussion:

1. What happened if the DC voltage in the clamping circuit is replaced by an a.c source?
2. What is the relationship between the clipping level and the DC voltage?
3. If the variable DC source is reversed, how does this affect the clipping?
4. If the input voltage $10_{VP.P}$, sketch the output of the circuit shown below.



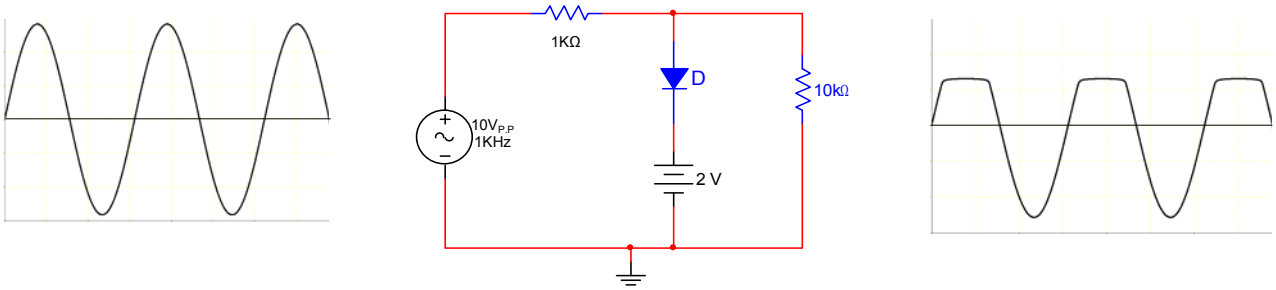


Fig. 1 Clipping circuit

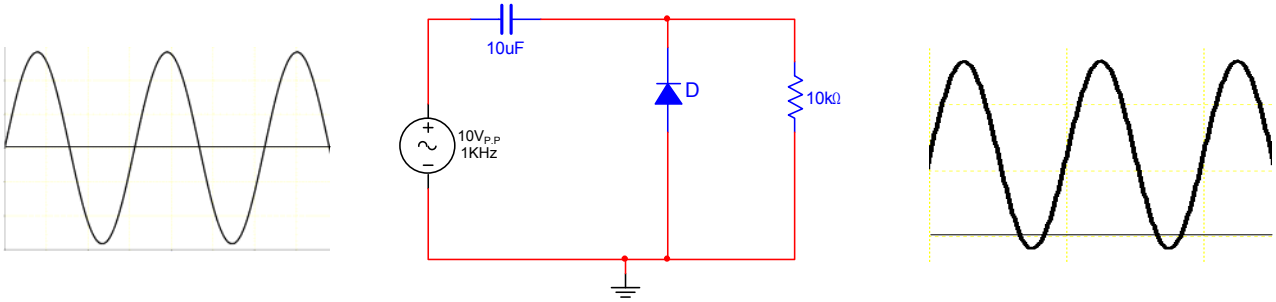


Fig. 2 Clamping circuit

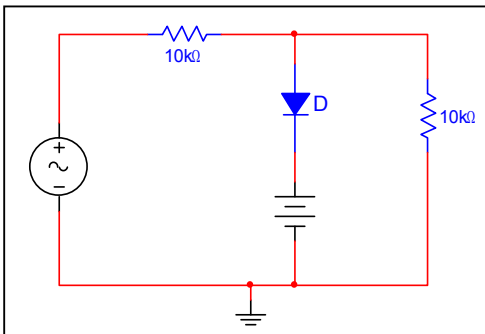


Fig. 3

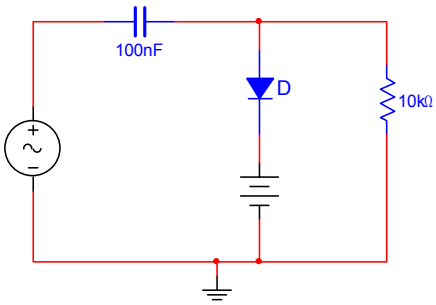


Fig. 4

Experiment No. 14

Common Base Amplifier

Object:

To examine the Common Base (CB) Amplifier characteristic of transistor.

Apparatus:

1. Two DC power supply.
2. Function generator.
3. AVOmeter.
4. Oscilloscope.
5. Transistor, Resistors 1 KΩ and 100 KΩ, Capacitors 1μf.

THEORY

Fig. 1 shows the circuit of a single-stage CB amplifier using NPN transistor.

As seen, input ac signal is injected into the emitter-base circuit and output is taken from the collector-base circuit. The E/B junction is forward-biased by V_{EE} where as C/B junction is reverse-biased by V_{CC}. The Q-point or dc working conditions are determined by dc batteries along with resistors R_E and R_C. In other words, values of I_E, I_B and V_{CB} are decided by V_{CC}, V_{EE}, R_E and R_C. The voltage V_{CB} is given by the equation $V_{CB}= V_{CC} – I_CR_C$.

When no signal is applied to the input circuit, the output just sits at the Q-point so that there is no output signal. Let us now see what happens when we apply an ac signal to the E/B junction via a coupling capacitor C_1 (which is assumed to offer no reactance to the signal).

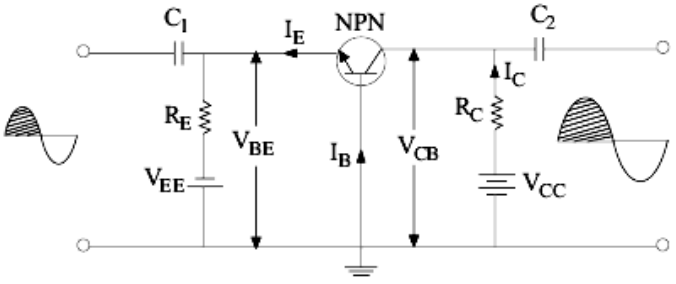


Fig. 1

Circuit Operation

When positive half-cycle of the signal is applied, then

1. forward bias is decreased because VBE is already negative with respect to the ground.

2. consequently, IB is decreased.

3. IE and hence IC are decreased (because they are both nearly β times the base current).
4. the drop IC RC is decreased.
5. hence, VCB is increased as seen by the equation given above

Common-base amplifier has

1. very low input resistance (30 – 150 Ω).
2. very high output resistance (up to 500 K).
3. a current gain $\alpha < 1$.
4. large voltage gain of about 1500.
5. power gain of up to 30 dB.
6. no phase reversal between input and output voltages.

Procedure:

1. Connect the circuit as shown in figure (2).
2. Measure Ic and Ie.
3. Draw output waveform on graph paper.

Discussion:

1. Determine Ai, Av, and Ap.
2. What is the effect of Re on amplifier?

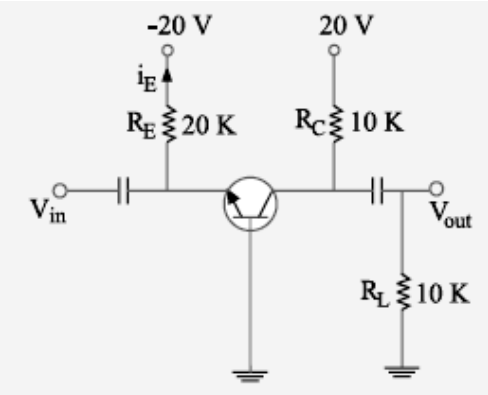


Fig. 2

Experiment No. 15
Common collector Amplifier

Object:

To examine the Common collector (CC) Amplifier characteristic of transistor.

Apparatus:

1. Two DC power supply.
2. Function generator.
3. AVOmeter.
4. Oscilloscope.
5. Transistor, Resistors 1 KΩ and 100 KΩ, Capacitors 1μf.

THEORY

Fig.1 and 2 show the circuit of a single-stage *CC* amplifier using an *NPN* transistor. The input signal is injected into the base-collector circuit and output signal is taken out from the emitter-collector circuit. The *E*/*B* junction is forward-biased by V_{EE} and *C*/*B* junction is reverse-biased by V_{CC}. The quiescent values of I_B and I_E are set by V_{CC} and V_{EE} together with R_B and R_E. As seen from Fig. 2.

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/\beta}$$

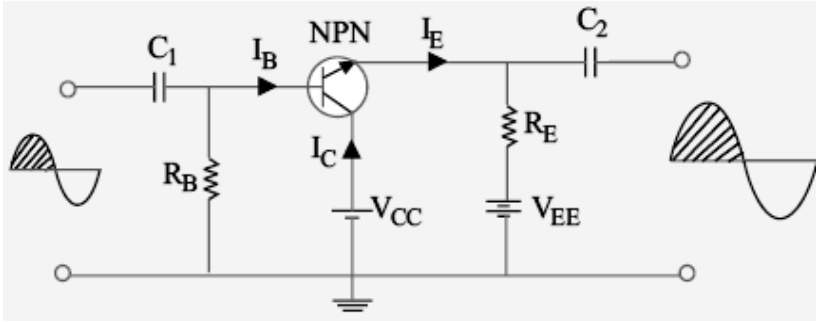


Fig. 1

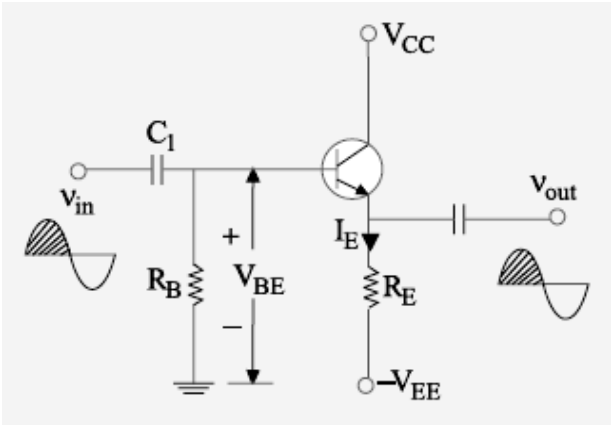


Fig. 2

Circuit Operation

When positive half-cycle of the signal is applied, then

1. forward bias is ***increased*** since V_{BE} is positive w.r.t. collector i.e. ground,

2. base current is ***increased***,

3. emitter current is ***increased***,

4. drop across R_E is ***increased***,

5. hence, output voltage (*i.e.* drop across R_E is ***increased***).

Consequently, we get positive half-cycle of the output. It means that a ***positive-going*** input signal results in a ***positive going*** output signal and, consequently, the input and output signals are in phase with each other as shown in Fig. 2.

Characteristics of a CC Amplifier

A *CC* amplifier has the following characteristics :

1. high input impedance (20-500 K),

2. low output impedance (50-1000 Ω),

3. high current gain of (1 + β) *i.e.* 50 – 500,

4. voltage gain of less than 1,

5. power gain of 10 to 20 dB,

6. no phase reversal of the input signal.

Procedure:

Consider the circuit shown in Fig. (3), it is a single stage amplifier

1- Connect the circuit.

2- Give an input to the amplifier so that the output is 4Vpp at 1 kHz Measure the input voltage (f=1 kHz).

3- Give an input of 0.5V p-p to the amplifier.

Discussion:

1. Determine Ai, Av, and Ap.
2. What is the effect of Rb on amplifier?

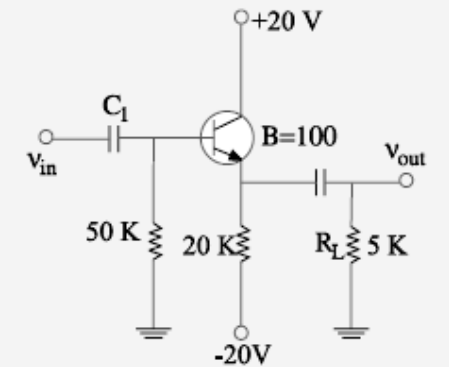


Fig. 3

Experiment No. 13
Common Emitter Amplifier

Object:

To examine the Common Emitter (CE) Amplifier characteristic of transistor.

Apparatus:

1. Two DC power supply.
2. Function generator.
3. AVOmeter.
4. Oscilloscope.
5. Transistor 2N2222, Resistors 1 KΩ and 100 KΩ, Capacitors 1µf.

THEORY

Fig. 1 and 2 show the circuit of a single-stage CE amplifier using an NPN transistor. Here, base is the driven element. The input signal is injected into the base emitter circuit whereas output signal is taken out from the collector emitter circuit. The E/B junction is forward-biased by VBB and C/B junction is reversed-biased by VCC (in fact, same battery VCC can provide dc power for both base and collector as in Fig. 2). The Q-point or working condition is determined by VCC together with RB and RC. The dc equation is (Fig. 2).

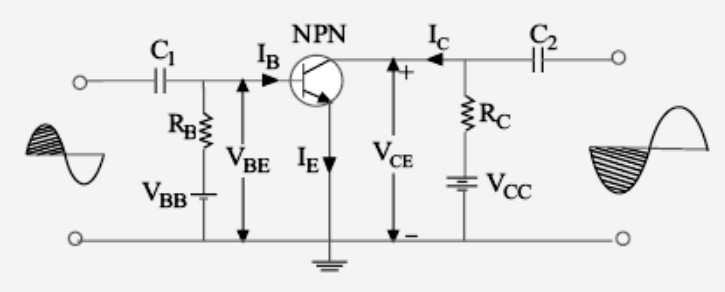


Fig. 1

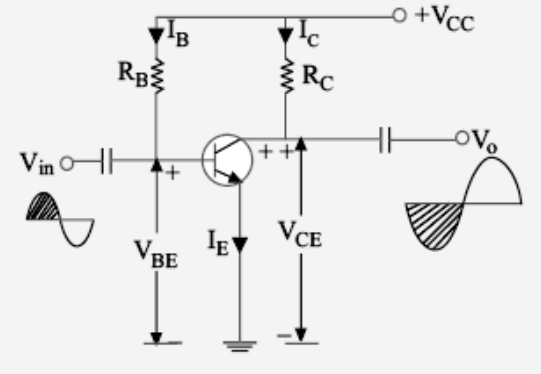


Fig. 2

Circuit Operations

When positive half-cycle of the signal is applied (Fig. 1)

1. *VBE* is increased because it is already positive w.r.t. the ground.
2. it leads to increase in forward bias of base emitter junction.

3. *IB* is increased somewhat.
4. *IC* is increased by α times the increased in *IB*.
5. drop *IC RC* is increased considerably and cons- equently.
6. *VCE* is decreased as seen from the equation given above.

Hence, negative half-cycle of the output is obtained. It means that a positive-going input signal becomes a negative going output signal as shown in Fig. 1 and 2.

Characteristics of a CE Amplifier

A *CE* transistor amplifier has the following characteristics :

1. it has moderately low input resistance (1 K to 2 K),
2. its output resistance is moderately large (50 K or so),
3. its current gain (β) is high (50–300),
4. it has very high voltage gain of the order of 1500 or so,
5. it produces very high power gain of the order of 10,000 times or 40 dB,
6. it produces *phase reversal* of input signal *i.e.* input and output signals are 180° out of phase with each other.

Procedure:

Consider the circuit shown in Fig. (3), it is a single stage amplifier

1- Connect the circuit.

2- Give an input to the amplifier so that the output is 4Vpp at 1 kHz Measure the input voltage (f=1 kHz).

3- Give an input of 0.5V p-p to the amplifier.

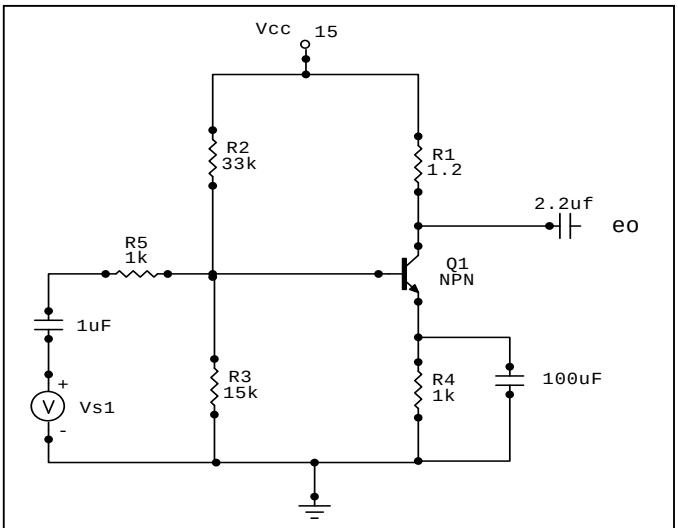


Fig.(3) Common Emitter Amplifier

Discussion:

1. Determine Ai, Av, and Ap.
2. What is the effect of Rb on amplifier?

Experiment No 2

Diode Rectifier and Smoothing Filters

Object:

To examine the basic diode rectifier systems and associated smoothing filters.

Apparatus:

1. Function Generator.
2. Oscilloscope.
3. AVOmeter.
4. Breadboard, Four Diodes, Two Capacitors and 1KΩ Resistor.

Introduction:

Almost all electric circuits require a DC source of power. A DC power supply is as equipment which converts the alternating waveform from the power lines into an essentially direct voltage. The power supply is composed of three main parts.

Rectifier, filter and Regulator (the regulator is not considered in this experiment). ***A rectifier*** is a device capable of converting a sinusoidal input waveform, whose average value is zero, into a unidirectional waveform with non zero average component. The rectifier device is usually a semiconductor or vacuum-tube diode. A smoothing filter is induced between the rectifier and load in order to attenuate the ripple component.

Theory:

Half wave rectification:

The basic circuit for half wave rectification is shown in Figure (l). The diode will conduct in the positive half cycle of sinusoidal input voltage $V_{in} = V_m \sin wt$. The current (i) in the diode and the load is given by:

$I = I_m \sin\alpha$ *when* $0 \le \alpha \le \pi$

$I = 0$ *when* $\pi \le \alpha \le 2\pi$

Where $I_m = \dfrac{V_m}{R_f + R_L}$

And R_f is the forward resistance of the diode. The average is shown in Figure (2).

The average value of the load current.

$$I_{d.c} = \frac{1}{2\pi}\int_0^{2\pi} i \cdot dt$$

The r.m.s value of the load current.

$$I_{rms} = \frac{1}{2\pi}\int_0^{2\pi} i^2 \cdot dt$$

The DC output voltage.

$$V_{d.c} = V_{d.c} \cdot R_L = \frac{I_m \cdot R_L}{\pi}$$

Ripple Factor:

The ripple factor is a measure of the fluctuating component in the output voltage and is defined as:

$$r = \frac{\text{rms value of alternative component of wave}}{\text{average value of wave}}$$

$$r = \frac{I_{rms} \cdot V_{rms}}{I_{dc} \cdot V_{dc}}$$

An expression for the ripple factor could be obtained, using the above definition in the following:

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1}$$

Full-wave rectification:

The circuit of the full-wave rectifier is shown in Figure (2).

From the definitions discussed above, the same quantities are found.

$$I_{dc} = \frac{2I_m}{\pi}, \qquad I_{rms} = \frac{I_m}{\sqrt{2}}$$

Where $I_m = \dfrac{V_m}{R_f + R_L}$

Procedure (Half-wave Rectifier):

1. Set up the half-wave rectifier shown in Figure (l) with R_L=1 KΩ.

2. Examine with the double-beam oscilloscope the input and output waveform .Draw the waveform to scale on the same time axis for input voltage 10 $V_{P.P}$, f =l KHz.
3. Measure the DC output V_{DC} with a DC voltmeter.
4. Measure the r.m.s value of the ripples voltages V_{rms} using an a.c voltmeter.
5. Connect a smoothing capacitor of l μf in shunt with load in Figure (l), Draw the input and output waveform.

Procedure (Full-wave Bridge Rectifier):

1. Connect the circuit shown in Figure (2).
2. Set the applied voltage to (10 $V_{P.P}$), (1 KHz).
3. Sketch the input and output waveform up to scale.
4. Measure V_{dc}, V_{rms} and calculate the ripple factor (*r*) for the value of R_L.
5. Connect the l μf smoothing capacitor across the load resistor and sketch the input and output waveforms.

Discussion:

1. Compare between theoretical and practical results, obtain for half-wave and full-wave rectifiers.
2. What is the value of the peak inverse voltage on the diode in full-wave rectifier?
3. Discuss the results obtained for full-wave circuit with capacitors filter.
4. What are the advantages and disadvantage of capacitor filters?

Figure (1)

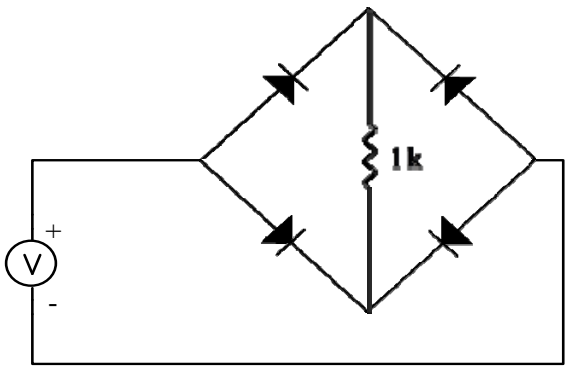


Figure (2)

Experiment No.12
Field Effect Transistor (FET)

OBJECT:

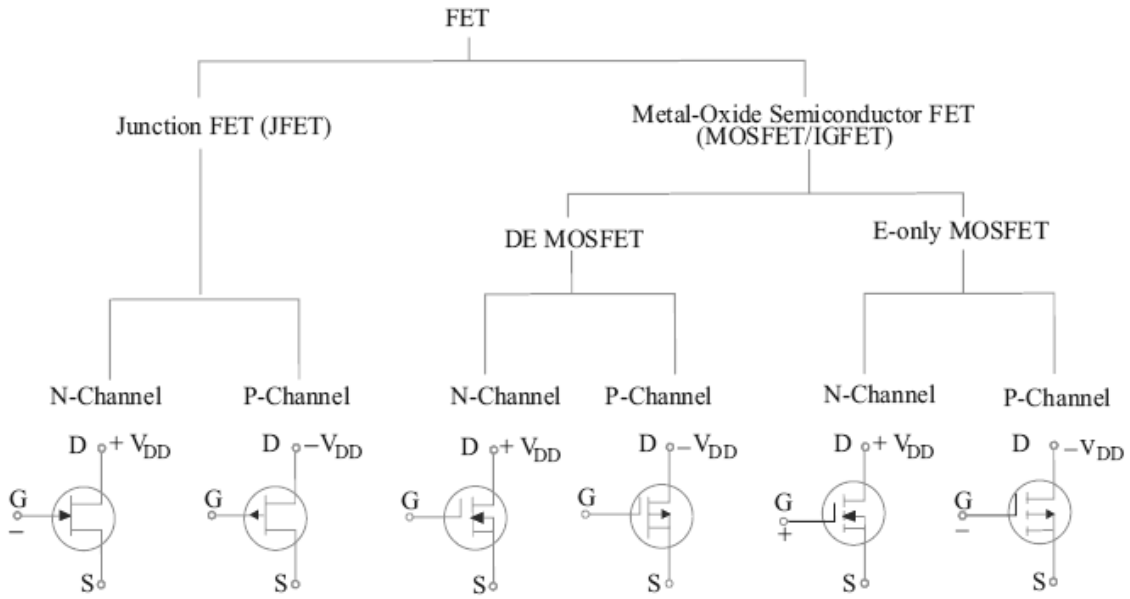
To investigate the FET characteristics .

APPARATUS:

1-D.C power supply .
2-Oscilloscope ,A.V.Ometer .
3-FET, Resistors 1kΩ and 200kΩ.

THEORY

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid-state device in which current is controlled ***by an electric field*** as is done in vacuum tubes. Broadly speaking, there are two types of FETs :
(*a*) junction field effect transistor (JFET)
(*b*) metal-oxide semiconductor FET (MOSFET)
It is also called insulated-gate FET (IGFET). It may be further subdivided into :
(*i*) depletion-enhancement MOSFET *i.e.* DEMOSFET
(*ii*) enhancement-only MOSFET *i.e.* E-only MOSFET
Both of these can be either *P*-channel or *N*-channel devices.
The FET family tree is shown below :



As shown in Fig.1, it can be fabricated with either an N-channel or P-channel though N-channel is generally preferred. For fabricating an N-channel JFET, first a narrow bar of N-type semiconductor material is taken and then two P-type junctions are diffused on opposite sides of its middle part [Fig.1 (a)]. These junctions form two P-N diodes or gates and the area between these gates is called channel. The two P-regions are internally connected and a single

lead is brought out which is called gate terminal. Ohmic contacts (direct electrical connections) are made at the two ends of the bar-one lead is called source terminal S and the other drain terminal D. When potential difference is established between drain and source, current flows along the length of the 'bar' through the channel located between the two P-regions. The current consists of only majority carriers which, in the present case, are electrons. P-channel JFET is similar in construction except that it uses P-type bar and two N-type junctions. The majority carriers are holes which flow through the channel located between the two N-regions or gates.

Following FET notation is worth remembering:

1. Source. It is the terminal through which majority carriers enter the bar. Since carriers come from it, it is called the source.
2. Drain. It is the terminal through which majority carriers leave the bar i.e. they are drained out from this terminal. The drain to source voltage V_{DS} drives the drain current I_D.
3. Gate. These are two internally-connected heavily-doped impurity regions which form two P-N junctions. The gate-source voltage V_{GS} reverse biases the gates.
4. Channel. It is the space between two gates through which majority carriers pass from source-to-drain when V_{DS} is applied.

Schematic symbols for N-channel and P-channel JFET are shown in Fig.1 (c). It must be kept in mind that gate arrow always points to N-type material.

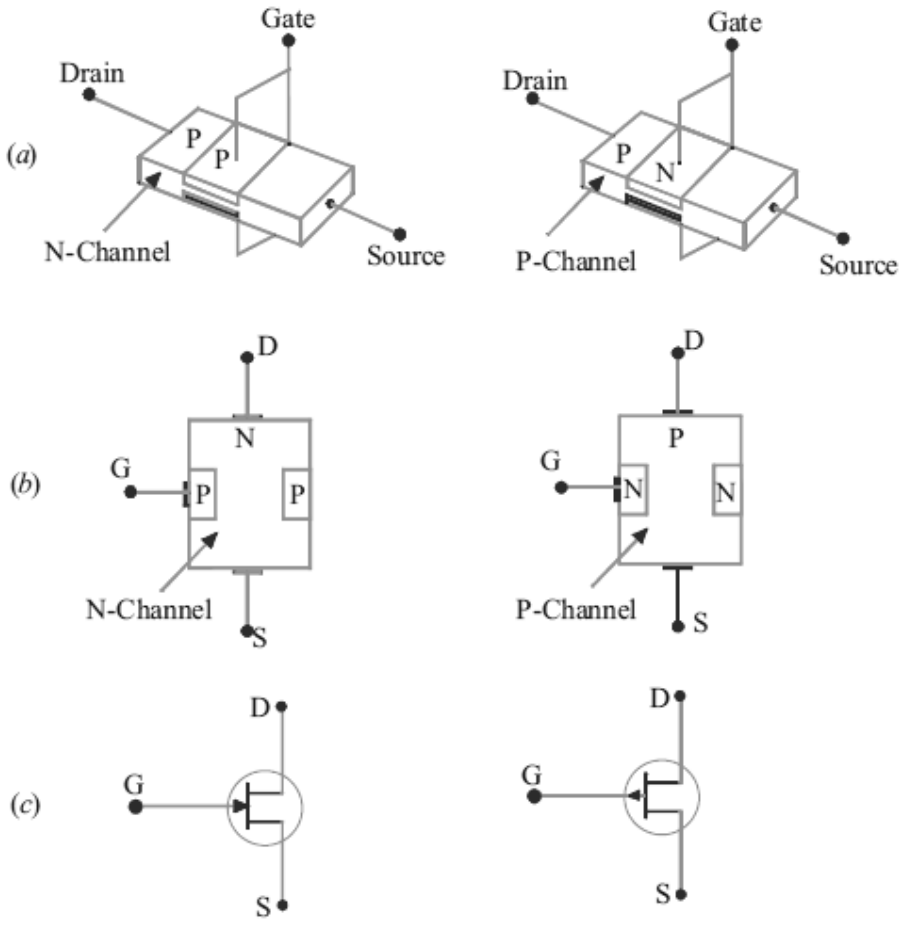


Fig. 1 FET construction

Static Characteristics of a JFET

We will consider the following two characteristics:

(i) drain characteristic: It gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).

(ii) transfer characteristic: It gives relation between I_D and V_{GS} for different values of V_{DS}.

We will analyze these characteristics for an N-channel JFET connected in the common-source mode as shown in Fig. 2. We will first consider the drain characteristic when $V_{GS}= 0$ and then when V_{GS} has any negative value upto V_{GS}(off).

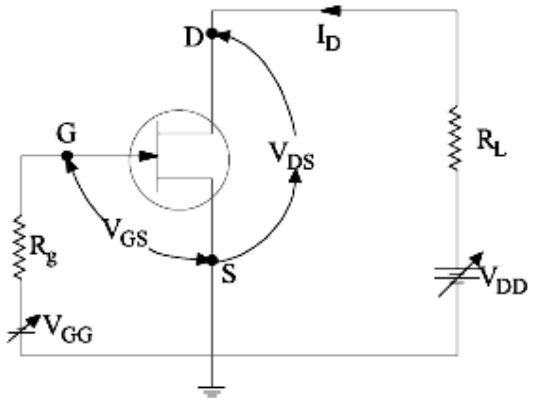


Fig. 2

JFET Drain Characteristic With $V_{GS} = 0$

Such a characteristic is shown in Fig. 3.

It can be subdivided into following four regions :

1. Ohmic Region OA: This part of the characteristic is linear indicating that for low values of V_{DS}, current varies directly with voltage following Ohm's Law. It means that JFET behaves like an ordinary resistor till point A (called knee) is reached.

2. Curve AB In this region, I_D increases at reverse square-law rate upto point B which is called pinch-off point. This progressive decrease in the rate of increase of I_D is caused by the square law increase in the depletion region at each gate upto point B where the two regions are closest without touching each other.

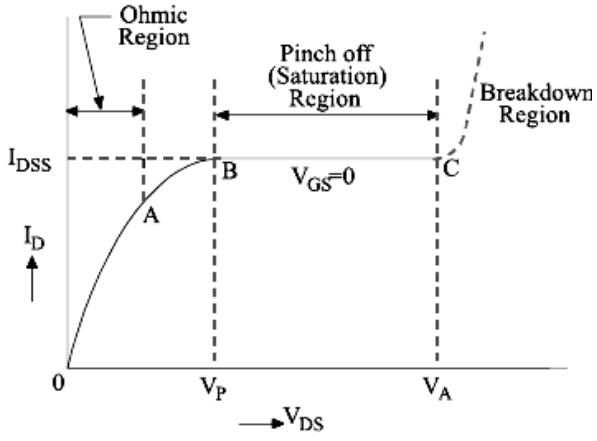


Fig. 3

3. Pinch-off Region BC: It is also known as saturation region or 'amplified' region. Here, JFET operates as a constant-current device because I_D is relatively independent of V_{DS}. It is due to the fact that as V_{DS} increases, channel resistance also increases proportionally thereby keeping I_D practically constant at I_{DSS}. It should also be noted that the reverse bias required by the gate-channel junction is supplied entirely by the voltage drop across the channel resistance due to flow of I_{DSS} and none by external bias because $V_{GS} = 0$.

4. Breakdown Region: If V_{DS} is increased beyond its value corresponding to point C (called avalanche breakdown voltage), JFET enters the breakdown region where I_D increases to an excessive value. This happens because the reverse-biased gate-channel P-N junction undergoes avalanche breakdown when small changes in V_{DS} produce very large changes in I_D. It is interesting to note that increasing values of V_{DS} make a JFET behave first as a resistor (ohmic region), then as a constant-current source (pinch-off region) and finally, as a constant-voltage source (breakdown region).

Procedure :

1- Connect the circuit as shown in fig 4.
2- Let V_{DS} =(0,0.5,1,1.5,2,2.5,3,4,5)v measure I_D.
3- Repeat step 3 for V_{GS} =(0.5,1,1.5,2,2.5,3,3.5,4,4.5) V.

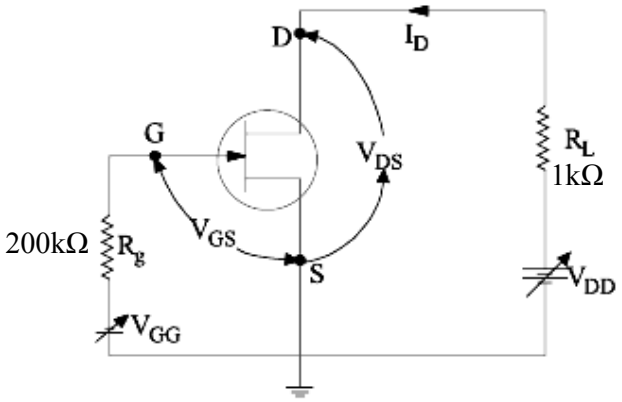


Fig. 4

REQUIREMENTS :

1- Draw (drain characteristics) between I_D & V_{DS} for different values of V_{GS}.
2- Draw I_D with V_{GS} & find gm .

DISCUSSION:

1-comment on your results.
2-compar between the transistor &FET .
3-what are the kind of FET .

Experiment No. 5

Input Characteristic of Transistor

Object:

To examine the input characteristic of transistor.

Apparatus:

1. Two DC power supply.
2. Three AVOmeters.
3. Transistor 2N2222, Resistor 1 KΩ, and Resistor 100 KΩ.

THEORY

There are six voltage and current parameters for transistor, as shown in figure (1). These six parameters are:

I_E The emitter current.

I_B The collector current.

I_C The base current.

V_{BE} The emitter-base voltage.

V_{BC} The base-collector voltage.

V_{EC} The emitter-collector voltage.

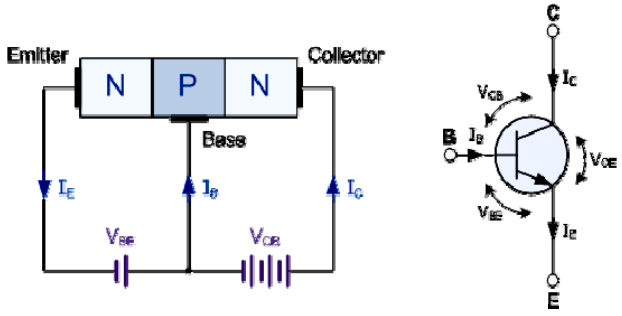


Figure (1) transistor parameters

By using Kirchhoff's laws, these parameters are related by the equation

$$I_E - I_B - I_C = 0$$

$$V_{EC} - V_{BC} - V_{BE} = 0$$

When any component is used in an electronic circuit it may represented as a box with an input and an output. The input and output must have terminals. This is shown in figure (2).

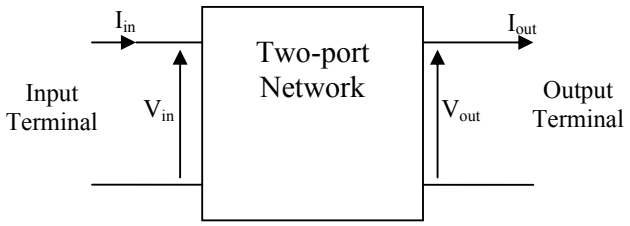
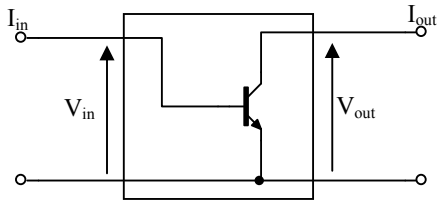


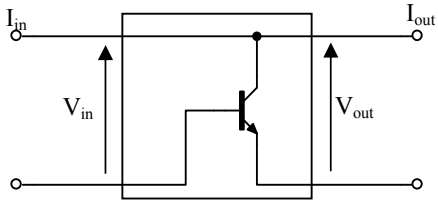
Figure (2) input and output terminals

The directions shown by the arrows are the conventional positive directions of the voltages and currents, e.g.; the input voltage is regarded as positive when terminal (1) is more positive than terminal (2), and the output current is regarded as positive when it flows into the output terminal. In a similar way transistor may be represented as a box, and mathematical relationship found between the input and output currents voltages. It is not necessary to know the actual component with the box if the mathematical equations of the box are known. These alone will specify how the component works in a circuit.

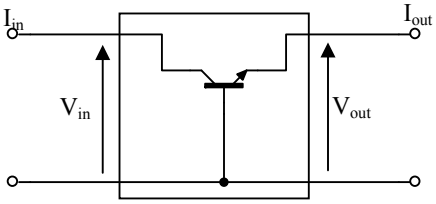
It is possible to have three different forms of connection of a transistor and these are shown in figure (3) As transistor is a device with three terminals, and the black-box always has four terminals (it is sometimes known terminal network), one of the transistor terminals to both input and output circuit.



a. common emitter



b. common collector



c. common base

Figure (3) transistor circuit connections

Hence the three connections in figure (3) may be denoted by the common terminal, as shown. Perhaps the most commonly used of the three circuit connections is that of the common emitter, as in figure (3a). In this connection

I_{in} is I_B

I_{out} is I_C

V_{in} is V_{BE}

V_{out} is V_{CE}

Figure (4) represents the linear portion of the input curve for a constant V_{CE}; the dotted curves represent input c/cs for different V_{CE}. The base-emitter voltage V_{BE}, depends on these factors I_B & V_{CE}; this can write in mathematical terms as:

$$\boldsymbol{V_{BE} = f\,(I_B\,,\, V_{CE})}$$

Or expressed in words: V_{BE} is a function of both I_B & V_{CE}, and its value depends on the values of both I_B and V_{CE}. It can be seen that the input curve have a slope, given by the change in V_{BE} divided by the corresponding change in I_B to produce it.

$$\boldsymbol{Slope = (V_{BE} / I_B)_{VCE\ constant}}$$

The input voltage is also dependent on V_{CE}, the output voltage. This relationship is given by the transfer c/cs curves.

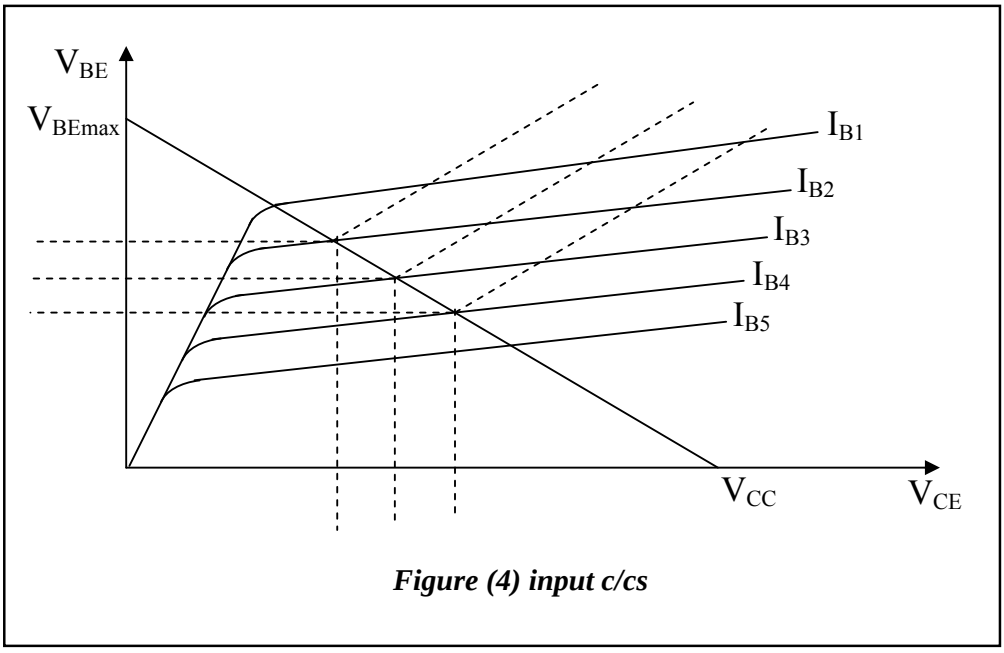


Figure (4) input c/cs

Procedure:

1. Connect the circuit shown in figure (5).
2. With I_B=0 & V_{CE} =0, record the value of V_{BE}.
3. Vary V_{BB} till the base current is 5 μA.
4. Repeat step 3 for base current of 10, 15, & 20 μA.
5. Repeat step 2 to 4 but for a value of V_{CE} equal to 0.2, 0.3 & 0.4 volt.
6. Tabulate your results in a table (1).
7. Draw input c/cs on graph paper.

Discussion:

1. Comment on the linearity of the curves.
2. Explain how the linear behavior of the transistor enables us to represent it by circuit of linear components.
3. From your graphs, find the four h-parameters.
4. Explain why the slope of the output c/cs. (hoe) is small.
5. From this experiment do you think that the transistor is a device which responds to, is sensitive to input voltage or input current?

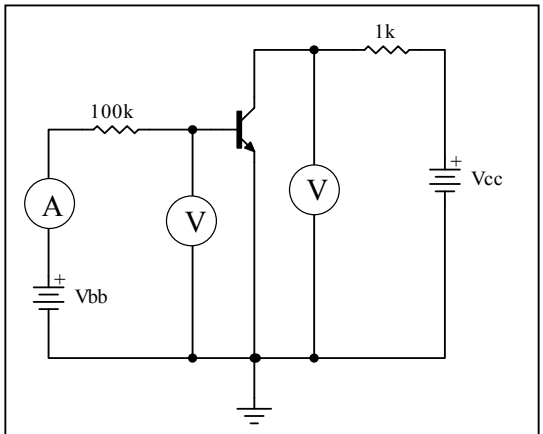


Figure (5) input c/cs circuit

V_{CE}	0	0.1	0.2	0.3	0.4
I_B	V_{BE}	V_{BE}	V_{BE}	V_{BE}	V_{BE}
0					
5					
10					
15					
20					

Table 1

EXPERIMENT NO. (11)

Integrator and Differentiator

OBJECT

To study the basic characteristics an applications of the operational amplifiers.

THEORY

The operational amplifier is a high gain high performance direct-coupled amplifier, which uses feedback to control its performance characteristics. Essentially, it consists of several transistor amplifiers. It is represented by the symbol shown in Fig.(1). It abbreviated as (Op Amp). Operational amplifiers are capable of amplify, controlling, generating sinusoidal or non-sinusoidal waveforms over frequencies from dc to MHz and computing operations such as (addition, subtraction, multiplication, integration, differentiation). Typical parameters of an operational amplifier (741) are:

Input resistance (R.) = 6 Mohm
Output resistance (R) = 70 Mohm
Open loop voltage gain (A) = 5000
Common mod rejection ratio (CMRR) = 90 db
Bandwidth (BU) = 1 MHz

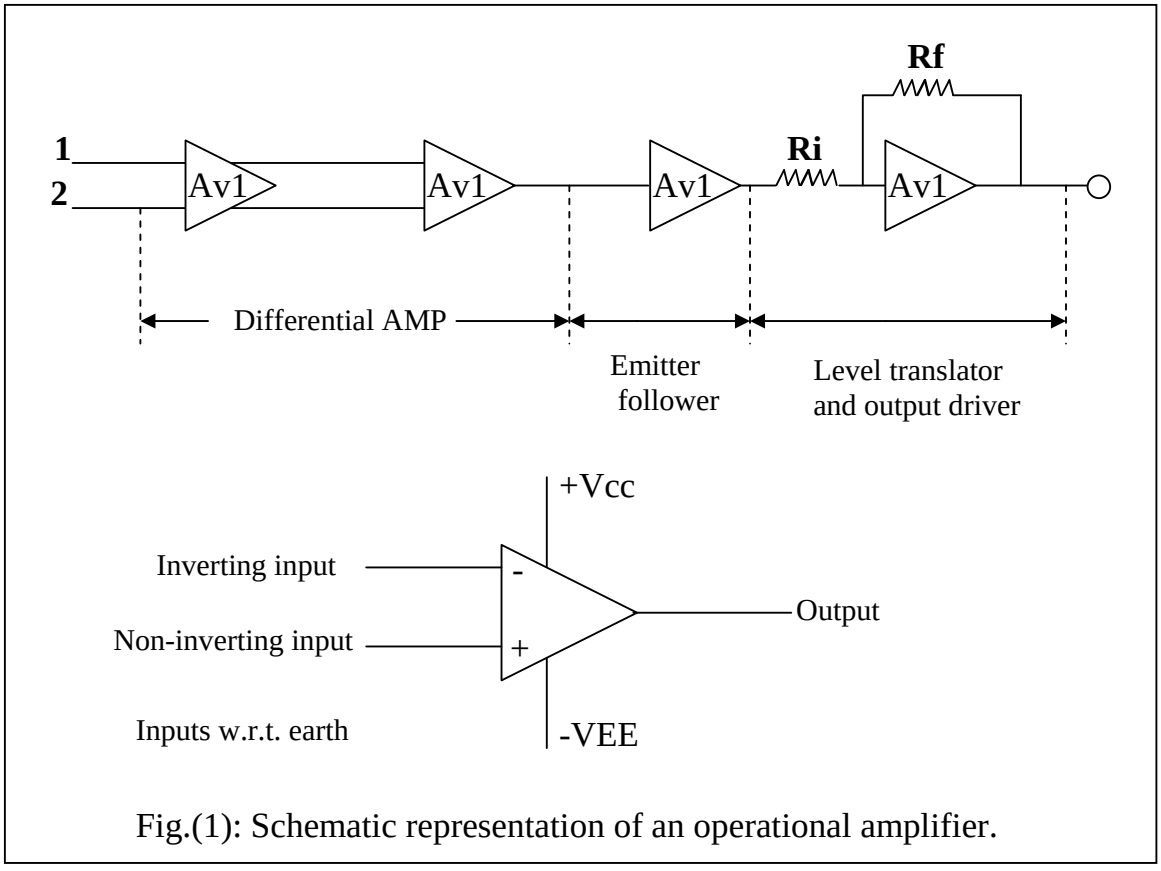


Fig.(1): Schematic representation of an operational amplifier.

PROCEDURE

1. Connect the circuit as shown in Fig.(2f) without capacitor. Apply a square wave signal of 1kHz, lV(p.p) to the input and observe the output waveform.
2. Connect a capacitor in parallel with resistance repeat step 9 for C=10nF.
3. Connect the circuit as shown in Fig.(2g). Apply a square wave to the input with a frequency of (1kHz) and amplitude 1V(p.p). Observe & draw the output waveform.

DISCUSSION

1. Discuss the characteristics of (OP AMP). State the differences between the inverting amplifiers.
2. Calculate the theoretical output for each of the above circuits and compare it with the experimental results?
3. Discuss the operation of the circuits shown in Fig.(2f) & Fig.(2g).
4. Discuss the effect of changing in the value of capacitor & frequency of input signal on the performance of the integrator & differentiator

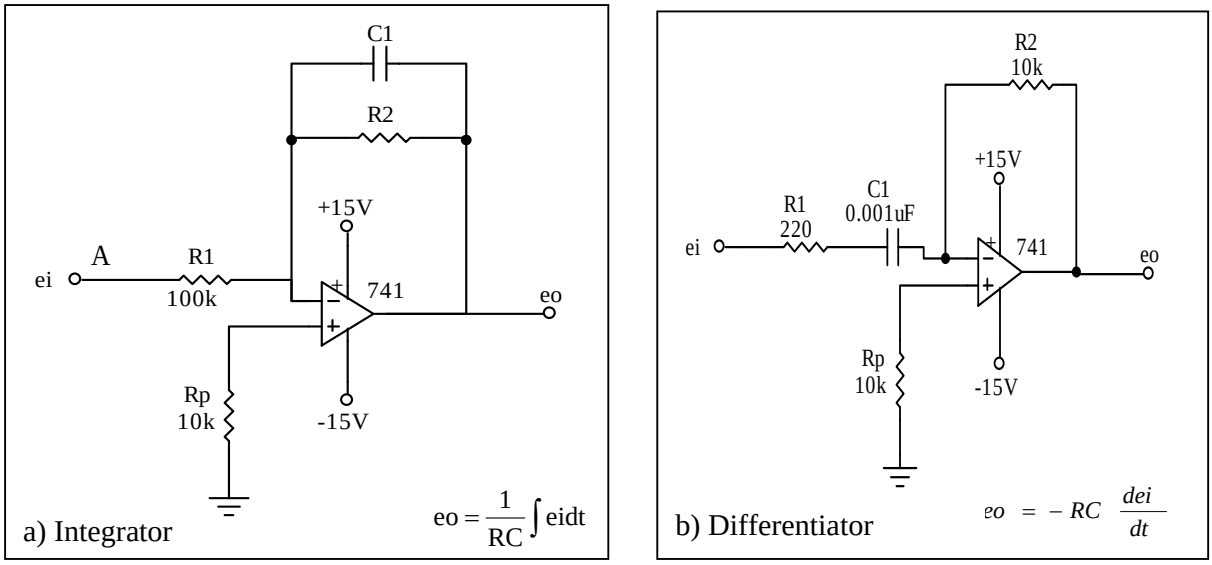


Fig. (2) Application of operational amplifier

Experiment No.7
Load line and Q-point

Object

To study the load line and operation point of basic transistor amplifier.

Apparatus

1. Dual DC power supply.
2. Function generator.
3. Oscilloscope.
4. Transistor 2N2222
5. bread board, resistors (100kΩ +100kΩ + 1kΩ) & capacitor 1μF
6. Two AVO meters.

Theory

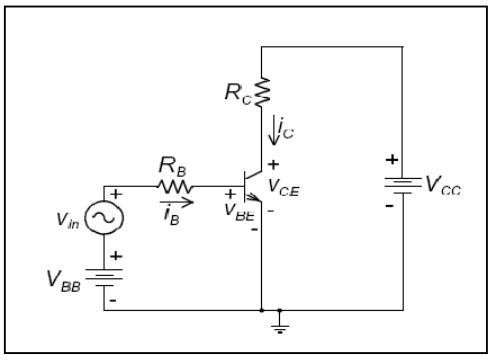
Basic BJT Common Emitter Circuit

1. Circuit Diagram and Equations

The basic BJT common emitter takes the form shown:

KVL equation around B-E loop: $$V_{BB} + v_{in} = i_B R_B + v_{BE}$$

KVL equation around C-E loop: $$V_{CC} = i_C R_C + v_{CE}$$



2. Load-Line Analysis - Input Side

Figure (1) shows the input characteristic of the transistor with input load line. Remember that the base-emitter is a *diode* and the *Thevenin resistance* is constant and *voltage* varies with time. Thus, the load line has constant slope (-1/*RB)*, and *moves with time*.

From Figure (1), It can be note that:

i. The load line shown for *Vin* = 0.

When *Vin* = 0, only dc remains in the circuit. This I_B, V_{BE} operating point is called the *quiescent point* (*Q-point)* is given special notation:

$\boldsymbol{I_{BQ}}$, $\boldsymbol{V_{BEQ}}$

ii. Maximum excursion of load line with V_{in} is shown in Figure (1)
iii. Minimum excursion of load line with V_{in} is shown in Figure (1).
Thus, as *Vin* varies through its cycle, base current varies from
i_{Bmax} to $i_{B\,min}$. The base-emitter voltage varies also, from $V_{BE\,max}$ to $V_{BE\,min}$.

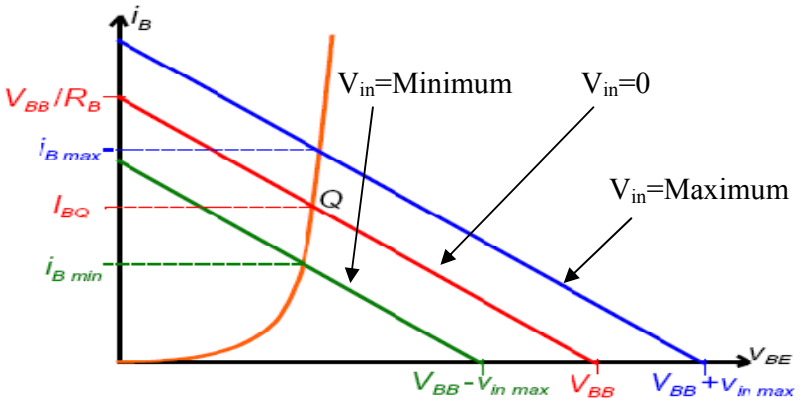


Figure (1): Load line on the input characteristics

3. ***Load-Line Analysis - Output Side***

Returning to the circuit, observe that V_{CC} and R_C form a Thevenin equivalent, with output variables I_C and V_{CE}. Thus we can plot this load line on the transistor *output characteristics,* because neither V_{CC} nor R_C are time-varying, this load line is fixed

1. The collector-emitter operating point is given by the intersection of the load line and the appropriate base current curve. When V_{in} = 0, $I_B = I_{BQ}$, and the quiescent point is I_{CQ}, V_{CEQ}. At $V_{in\,max}$, $I_B = I_{B\,max}$, and the operating point is $I_{C\,max}$, $V_{CE\,min}$. At $V_{in\,min}$, $I_B = I_{B\,min}$, and the operating point is $I_{C\,min}$, $V_{CE\,max}$.
2. If the total change in V_{CE} is greater than total change in V_{in}, we have an *amplifier*

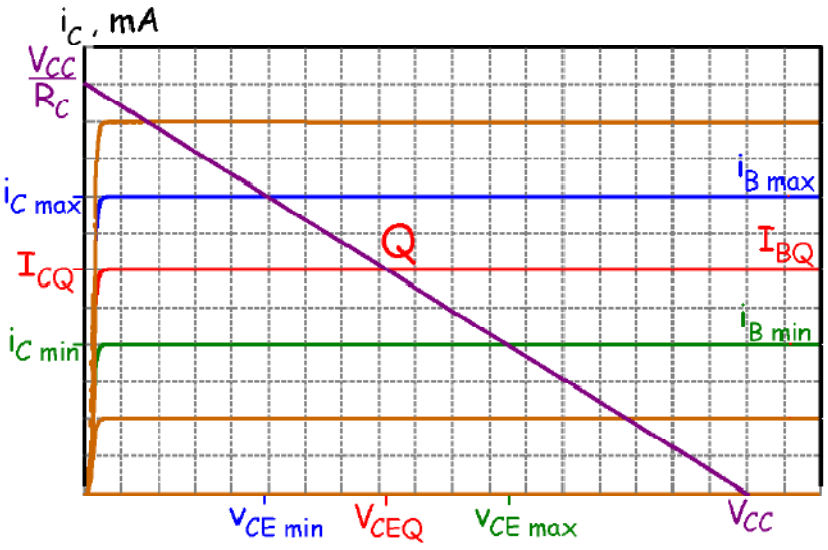


Figure (2): DC load line on the output characteristics

Procedure

1. Connect the circuit shown in Figure(3)
2. With v_{in}= 0, vary the V_{BB} to obtain the I_C according to the Table (1). Then record the values of the V_{CE}.
3. Set the input voltage (v_{in}) to the value that obtain the maximum swing on the output voltage (v_{CE}).when the operating point in the middle of the load line.
4. Vary the biasing voltage V_{BB} to obtain the I_C = (2, 5 and 8) mA. Then plot the output voltage of each value.

I_C (mA)	0	2	4	5	6	8	10
V_{CE} (V)							

Table (1)

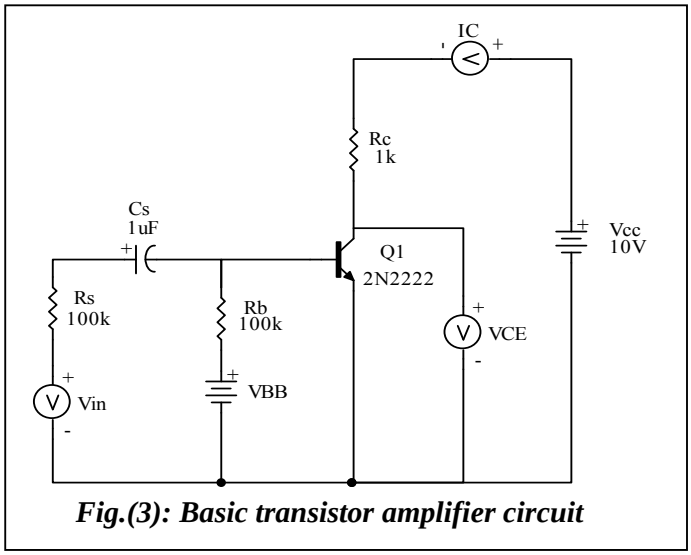
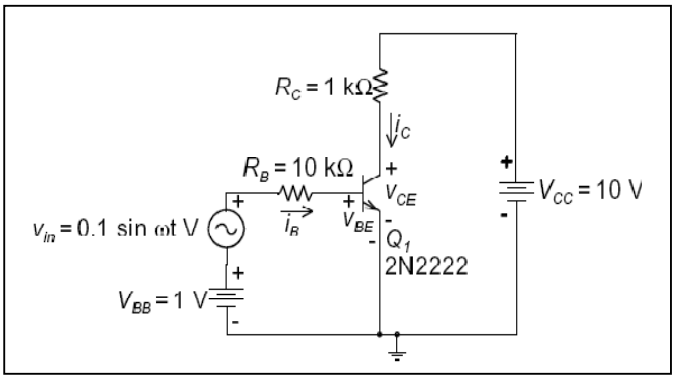


Fig.(3): Basic transistor amplifier circuit

Discussion

1. Plot the load line of the transistor according to the result.
2. Explain linearity of the load lines.
3. If the swing of the input current is reduced to the one half of the used value in the experiment, plot the output voltage at I_C= (2, 5 & 8) mA.
4. For the circuit shown below, find the Q-point (I_{CQ} & V_{CEQ}), $V_{CE\ min}$, $V_{CE\ max}$, $I_{C\ max}$ & i_{Cmin}. Then plot v_{in} & V_{CE}.



EXPERIMENT NO. (10)

Operational Amplifiers

OBJECT

To study the basic characteristics an applications of the operational amplifiers.

THEORY

The operational amplifier is a high gain high performance direct-coupled amplifier, which uses feedback to control its performance characteristics. Essentially, it consists of several transistor amplifiers. It is represented by the symbol shown in Fig.(1). It abbreviated as (Op Amp). Operational amplifiers are capable of amplify, controlling, generating sinusoidal or non-sinusoidal waveforms over frequencies from dc to MHz and computing operations such as (addition, subtraction, multiplication, integration, differentiation). Typical parameters of an operational amplifier (741) are:

Input resistance (R.) = 6 Mohm
Output resistance (R) = 70 Mohm
Open loop voltage gain (A) = 5000
Common mod rejection ratio (CMRR) = 90 db
Bandwidth (BU) = 1 MHz

EQUIPMENT

1. Signal generator
2. Dual power supply
3. Oscilloscope
4. OP AMP

PROCEDURE

1. Connect the circuit as Shown in Fig.(2a). choose Rl =10kohm & R2=100kohm, connect input terminals to earth and measure the output voltage eo. If eo is not equal to zero, vary balance potentiometer to obtain output voltage zero.
2. Connect ac voltage (5 KHz) or dc to one of the input and connect the other input to the earth and adjust the input amplitude to obtain output voltage as 4 volts. Measure el and e2.
3. Design an inverting amplifier Fig.(2b) to have gain=10 and input resistance to have at least 10kohm (R1=10kohm).
4. Connect the designed circuit. Measure dc gain then connect capacitor of (1 μF) at the input & output. Draw frequency response characteristics of the amplifier by measuring gain at 10, 100, 500, 5k, 20k, 50k, 100k, 300k, 500k, 800k, and 900k. Determine half power point frequencies (f1&fh) and bandwidth. .
5. Design a non-linear amplifier Fig.(2c) to have gain=11 and input resistance to have at least 10kohm and repeat step(4)
6. Design a summing amplifier Fig.(2d) Which provides an output voltage eo = 10(el + e2). Measure output voltage for el=O.5Volt & e2=l volt.

7. Observe and draw waveform of output voltage if el=O.5volt(p.p) sinewave of 500Hz & e = 0.5Vdc.
8. Connect the circuit as shown in Fig.(2e). Measure output voltage for e_{ref}= 1V and e_{in}=0.5V, 0.95V, 1.05V, and 1.3V.

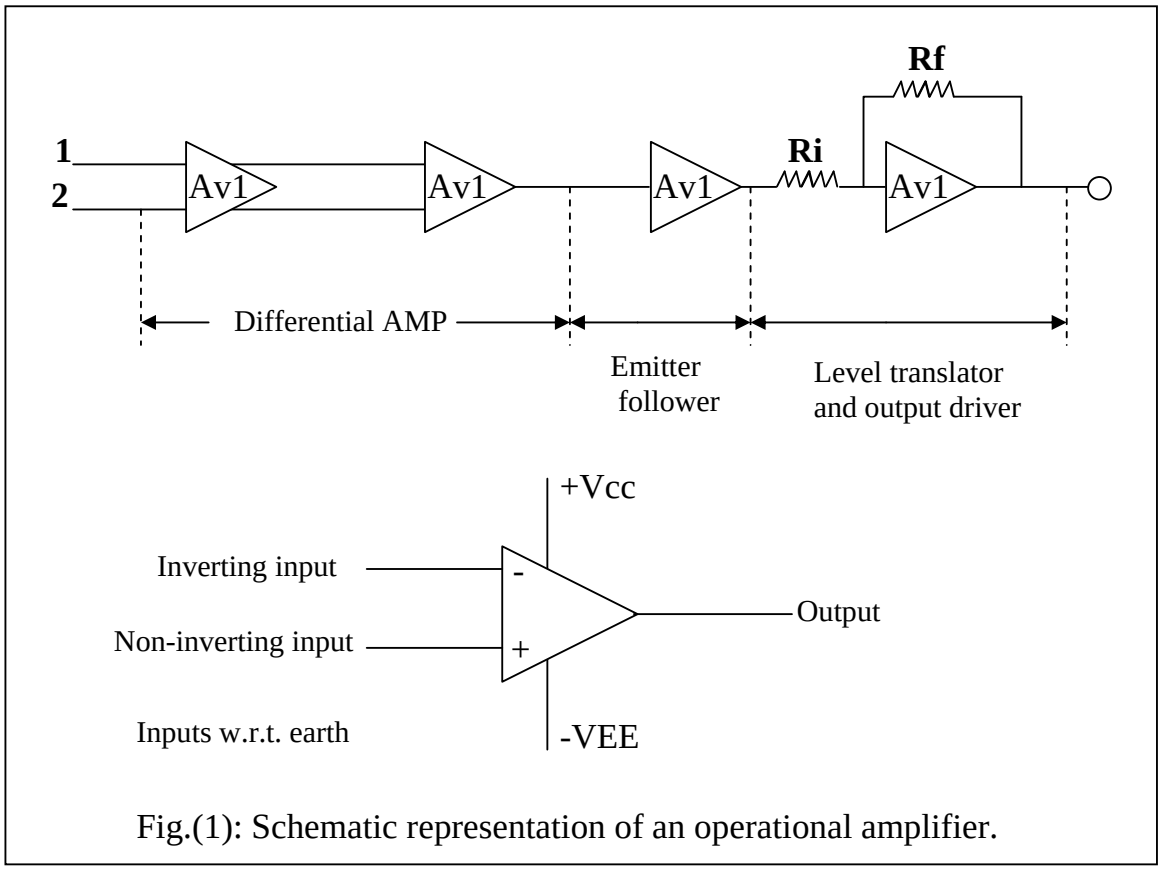
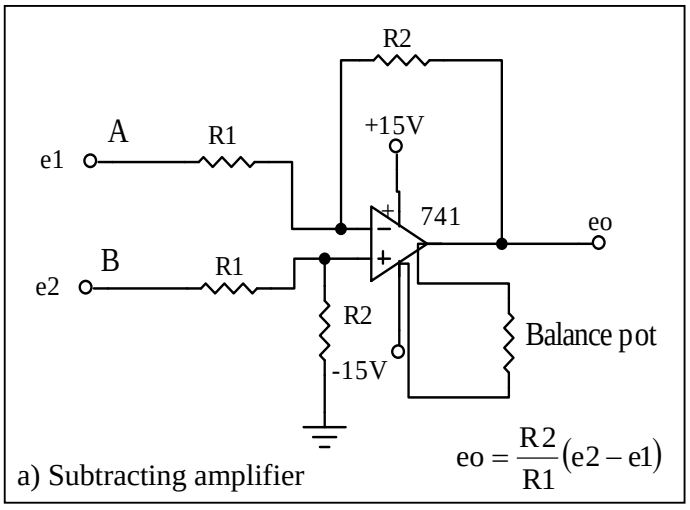


Fig.(1): Schematic representation of an operational amplifier.

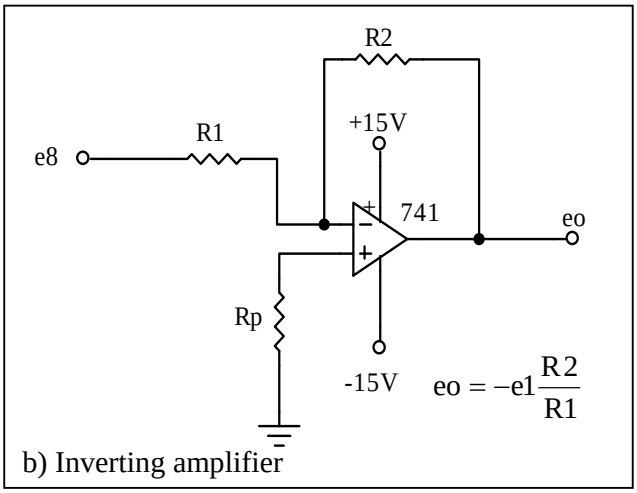
DISCUSSION

1. Discuss the characteristics of (OP AMP). State the differences between the inverting amplifiers.
2. Calculate the theoretical output for each of the above circuits and compare it with the experimental results?



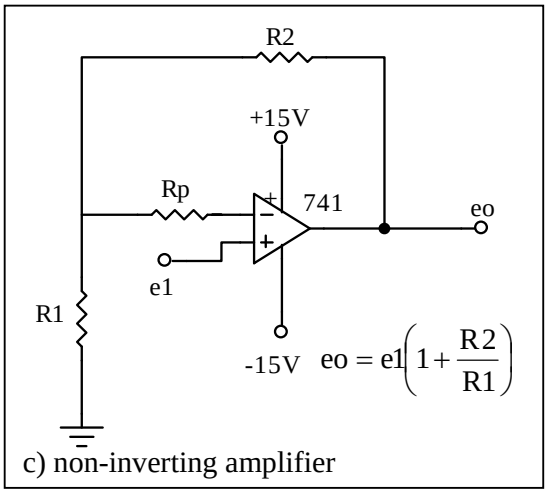
a) Subtracting amplifier

$$eo = \frac{R2}{R1}(e2 - e1)$$



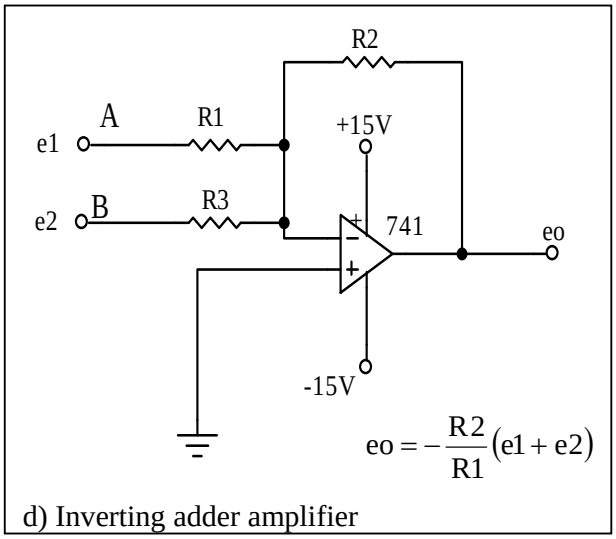
b) Inverting amplifier

$$eo = -e1\frac{R2}{R1}$$



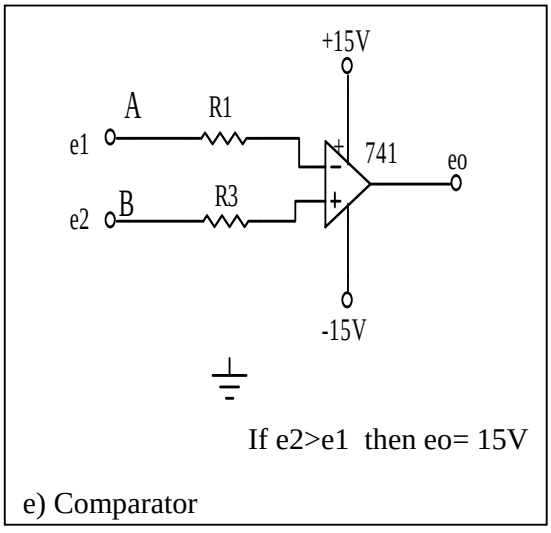
c) non-inverting amplifier

$$eo = e1\left(1 + \frac{R2}{R1}\right)$$



d) Inverting adder amplifier

$$eo = -\frac{R2}{R1}(e1 + e2)$$



If e2>e1 then eo= 15V

e) Comparator

Experiment No. 6

Output Characteristic of Transistor

Object:

To examine the output characteristic of transistor.

Apparatus:

1. Two DC power supply.
2. Three AVOmeters.
3. Transistor 2N2222, Resistor 1 KΩ, and Resistor 100 KΩ.

THEORY

There are six voltage and current parameters for transistor, as shown in figure (1). These six parameters are:

I_E The emitter current.

I_B The collector current.

I_C The base current.

V_{BE} The emitter-base voltage.

V_{BC} The base-collector voltage.

V_{EC} The emitter-collector voltage.

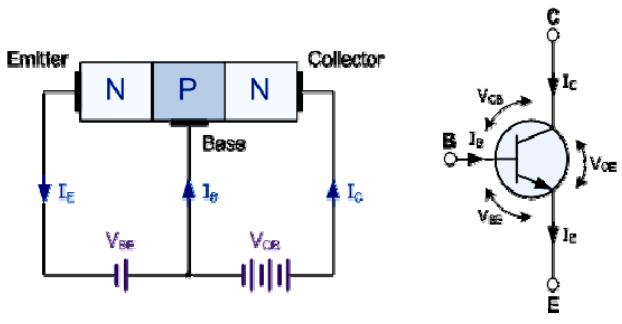


Figure (1) transistor parameters

By using Kirchhoff's laws, these parameters are related by the equation

$$I_E - I_B - I_C = 0$$

$$V_{EC} - V_{BC} - V_{BE} = 0$$

When any component is used in an electronic circuit it may represented as a box with an input and an output. The input and output must have terminals. This is shown in figure (2).

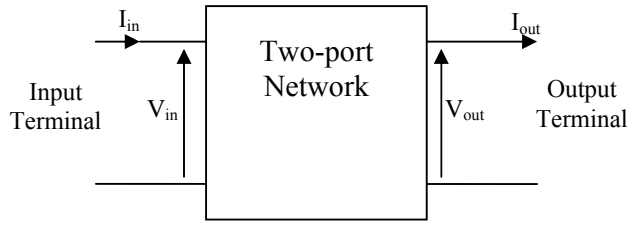
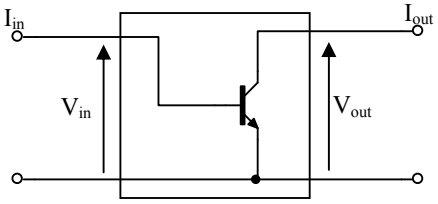


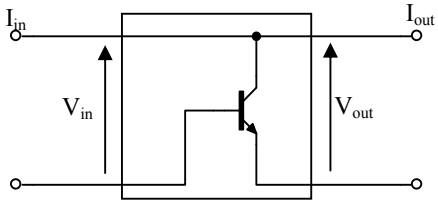
Figure (2) input and output terminals

The directions shown by the arrows are the conventional positive directions of the voltages and currents, e.g.; the input voltage is regarded as positive when terminal (1) is more positive than terminal (2), and the output current is regarded as positive when it flows into the output terminal. In a similar way transistor may be represented as a box, and mathematical relationship found between the input and output currents voltages. It is not necessary to know the actual component with the box if the mathematical equations of the box are known. These alone will specify how the component works in a circuit.

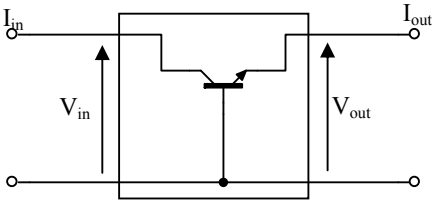
It is possible to have three different forms of connection of a transistor and these are shown in figure (3) As transistor is a device with three terminals, and the black-box always has four terminals (it is sometimes known terminal network), one of the transistor terminals to both input and output circuit.



a. common emitter



b. common collector



c. common base

Figure (3) transistor circuit connections

Hence the three connections in figure (3) may be denoted by the common terminal, as shown. Perhaps the most commonly used of the three circuit connections is that of the common emitter, as in figure (3a). In this connection

I_{in} is I_B

I_{out} is I_C

V_{in} is V_{BE}

V_{out} is V_{CE}

Figure (4) represents the linear portion of the output curve for a constant V_{CE}; the dotted curves represent input c/cs for different V_{CE}. The collector current I_C, depends on these factors I_B & V_{CE}; this can write in mathematical terms as:

$$\boldsymbol{I_C = f\,(I_B\,,\,V_{CE})}$$

Or expressed in words: I_C is a function of both I_B & V_{CE}, and its value depends on the values of both I_B and V_{CE}. It can be seen that the input curve have a slope, given by the change in I_C divided by the corresponding change in I_B to produce it.

$$\boldsymbol{Slope = (I_C / I_B)_{VCE\ constant}}$$

The input voltage is also dependent on V_{CE}, the output voltage. This relationship is given by the transfer c/cs curves.

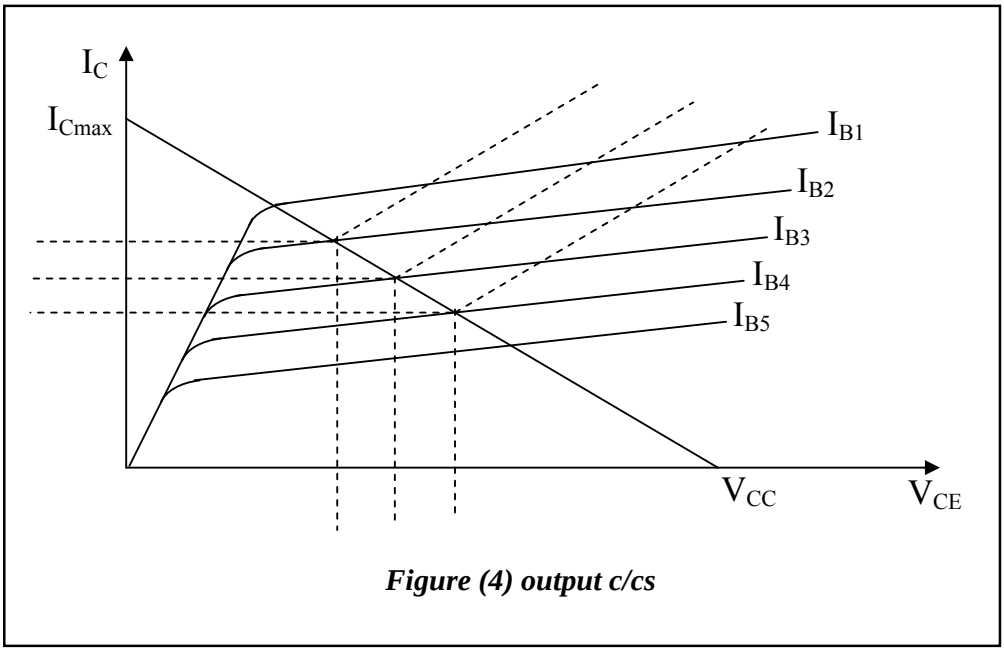


Figure (4) output c/cs

Procedure:

1. Connect the circuit as shown in figure (5).
2. Vary V_{BB} till the base current is 2.5 μA and V_{CE} =0, record the value of I_C.
3. Repeat step 2 for a value of V_{CE} equal to 0.25, 0.5, 1, 2, 3, 5, 10 volt.
4. Repeat step 3 but for base current of 5, 10, 15, & 20 μA.
5. Tabulate your results in a table (1).
6. Draw output c/cs on graph paper.

Discussion:

1. Comment on the linearity of the curves.
2. Explain how the linear behavior of the transistor enables us to represent it by circuit of linear components.
3. From your graphs, find the four h-parameters.
4. Explain why the slope of the output c/cs. (hoe) is small.
5. From this experiment do you think that the transistor is a device which responds to, is sensitive to input voltage or input current?

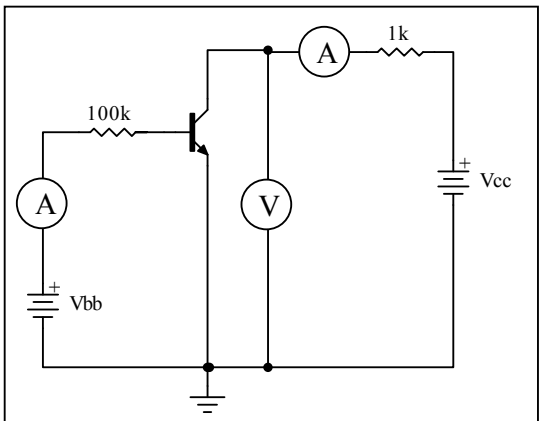


Figure (5) output c/cs circuit

I_B	2.5	5	10	15	20
V_{CE}	I_C	I_C	I_C	I_C	I_C
0.25					
0.5					
1					
2					
3					
5					
10					

Table 1

Experiment No.1

Semiconductor diode characteristics

Object:

To study the characteristics of the forward and reverse biased junction diodes.

Apparatus:

1. DC power supply.
2. Two AVOmeters.
3. Breadboard, Diode and 1KΩ Resistor.

Theory:

The general from of the current - voltage c/cs of a diode is shown in Figure (l). A current flow in the forward direction is very large compared with that in the reverse direction and such a device is very useful as a rectifier.

The diode is in the forward direction when an external battery is connected with positive

terminal to the (p) region and negative terminal to the region (n). The reverse current through the diode varies greatly with temperature and with the semiconductor materiel used.

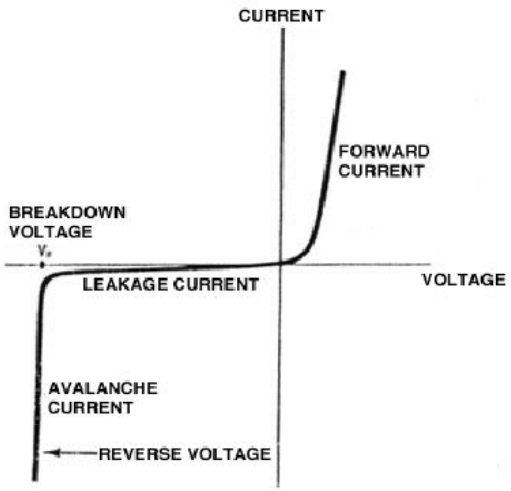


Figure (1) V-I c/cs of a real diode

Procedure:

1. Connect the circuit as shown in Figure (2) using silicon diode.
2. Increase the variable DC voltage from zero in steps of (0.1 volts) up to (1 volts), then in step of (0.5 volt) up to (4 volt), and record the voltage across the (100 ohm) resistance (Vr).
3. Tabulate your results in a table as shown in table (1).
4. Connect the circuit shown in Figure (3) using Si diode.
5. Increase the variable DC voltage from zero in steps of (0.2 volts) up to (1 volt), then in steps of (1 volt) up to (4 volts) and for each step record the current lowing in the circuit.
6. Tabulate your result in a table as shown in table (2).

Note:

For the reverse c/cs of (Si) diode the reverse current is very small compare with the current of (Ge) diode , so its assumed to be zero.

Discussion:

1. Compare between the Si & Ge diode? which is has the better forward c/cs?
2. What is the barrier field and how is it produce?
3. Comment on the results of the experiment.

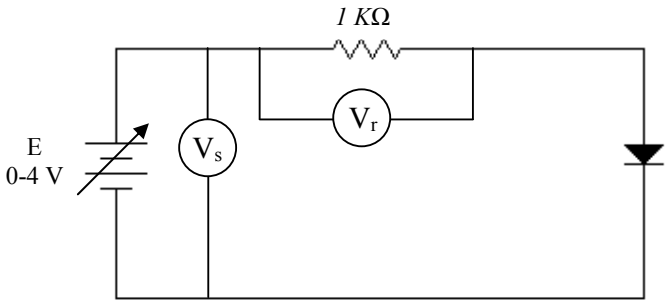
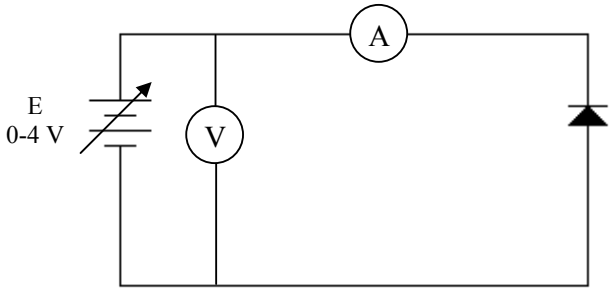


Figure (2) forward c/cs circuit

V_s (Volt)	V_r (Volt)	$V_f = V_s - V_r$ (Volt)	$I_f = V_r / r$ (mA)

Table (1)



Figure(3) Reverse c/cs circuit

$V_{reverse}$	$I_{reverse}$

Table (2)

Experiment No. 8
Transistor Biasing and Bias Stability

Aim of experiment:

To study the Transistor biasing types and bias stability.

Theory

Notice from the previous load line experiment (Experiment No.6)

1. The instantaneous operating point moves with instantaneous signal voltage. Linearity is best when operating point stays within the active regions.
2. The quiescent point is the dc (zero signal) operating point. It lies near the "middle" of the range of instantaneous operating points. This dc operating point is *required* if linear amplification is to be achieved!!!
3. The dc operating point (the *quiescent point*, the *Q point*, the *bias point*) obviously requires that dc sources be in the circuit.
4. The process of establishing an appropriate bias point is called *biasing* the transistor.
5. Given a specific type of transistor, biasing should result in the same or nearly the same bias point in every transistor of that type . . . this is called *bias stability*.

Bias stability can also mean stability with temperature, with aging, etc.

Transistor Biasing

1. The Fixed Bias Circuit

Fig.(1)shows the fixed biasing transistor circuit. The resistor R_B is supplied from Vcc directly then the I_B (D.C base current) is fixed at certain value. Therefore;

$$I_B = \frac{V_{CC} - V_{BE}}{R_b}$$

The following example explains the fixed biasing circuit stability.

Example

We let *VCC* = 15 V, RB = 200 kΩ, and *RC* = 1 kΩ and *β* varies from 100 to 300. To perform the analysis, we assume that operation is in the active region, and that *VBE* = 0.7 V.

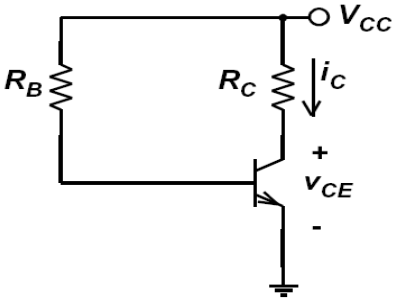


Fig.(1): Fixed Biasing circuit

For β= 100:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\text{ V} - 0.7\text{ V}}{200\text{k}\Omega} = 71.5\mu\text{A}$$

$$I_C = \beta I_B = 7.15\text{ mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C = 7.85\text{ V}$$

Q. Active region??? $V_{CE} > 0.7$ V and $I_B > 0$ *Yes!!!*

For β = 300:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{15\text{ V} - 0.7\text{ V}}{200\text{k}\Omega} = 71.5\ \mu\text{A}$$

$$I_C = \beta I_B = 21.5\text{mA} \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C = -6.45\text{ V}$$

Q. Active region??? $V_{CE} < 0.7$ V ***No!!!*** ***Saturation!!!***

Thus our calculations for *β*= 300 are incorrect, but more importantly. We conclude that fixed bias provides *extremely poor bias stability!!!*

2. The Constant Base Bias Circuit

A circuit which is used to establish a stable point is the constant base-biasing configuration of Fig.(2). The current in the resistance R_E in the lead is always constant. Therefore;

$$I_E = \frac{V_{BB} - V_{BE}}{R_E}$$

The following example explains the fixed biasing circuit stability.

Example

Now we let V_{CC} = 15 V and V_{BB} = 5 V, R_C = 2 kΩ and R_E = 2 kΩ β varies from 100 to 300. We assume operation in active region and *VBE* = 0.7 V, as before.

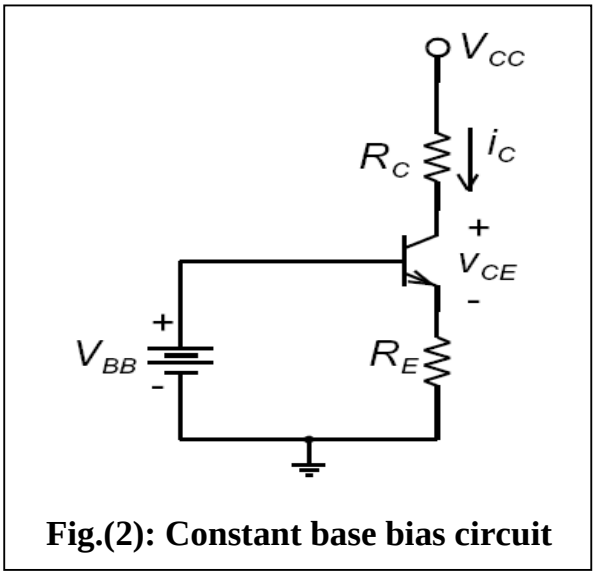


Fig.(2): Constant base bias circuit

For β = 100:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} = 2.15\ \text{mA} \quad \Rightarrow \quad I_C = \frac{\beta}{\beta + 1} I_E = 2.13\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.44\ \text{V}$$

For β = 300:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E} = 2.15\ \text{mA} \quad \Rightarrow \quad I_C = \frac{\beta}{\beta + 1} I_E = 2.14\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.41\ \text{V}$$

Thus we conclude that *constant base bias provides excellent bias stability!!!* Unfortunately, we can't easily couple a signal into this circuit, so it is not as useful as it may first appear.

3. The Four-Resistor Bias Circuit (Self –Biasing Circuit)

A circuit which is used to establish a stable operating point is the self-biasing confirmation of Fig.(3-a). The current in the resistance R_E in the emitter lead causes a voltage drop which is in the direction to reverse-bias the emitter junction. Since this junction must be forward-biased, the base voltage is obtained from he supply through the R_1& R_2 network.

Now, if I_C tends to increase, say, because I_{CO} has rise as a result of an elevated temperature, the current in R_E increases. Hence I_C will increase less than it would have, had there been no self-biasing resistor R_E.

This combines features of fixed bias and constant base bias, but it takes a circuit-analysis "trick" to see that in Fig.(3-b):

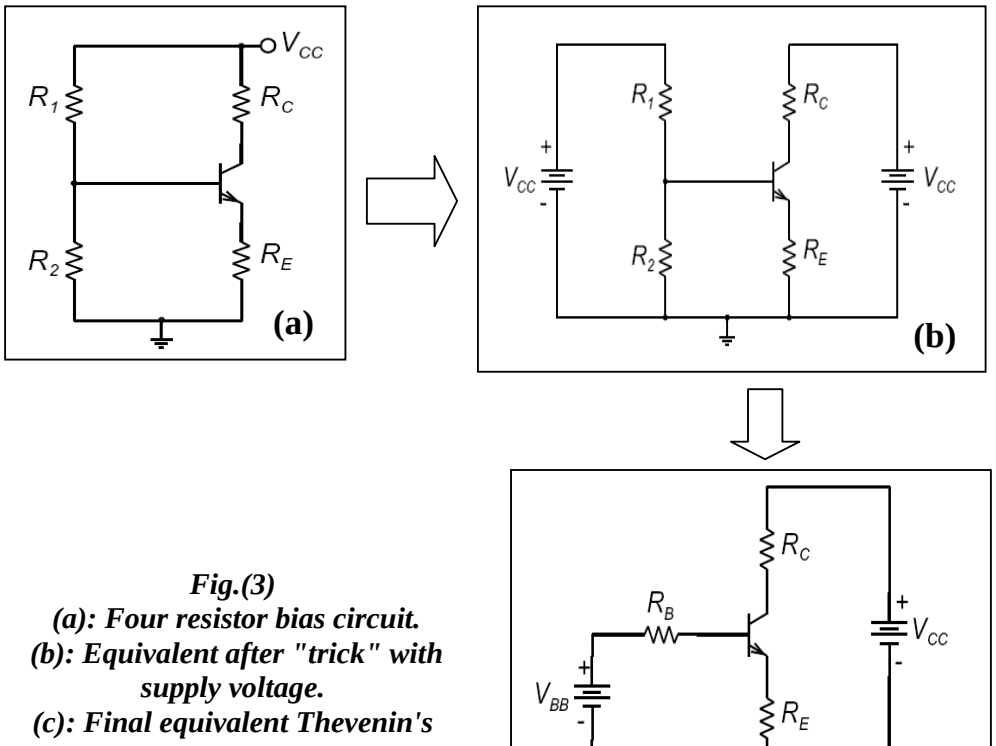


Fig.(3)
(a): Four resistor bias circuit.
(b): Equivalent after "trick" with supply voltage.
(c): Final equivalent Thevenin's

Circuit Analysis

Analysis begins with KVL around B-E loop:

$$V_{BB} = I_B R_B + V_{BE} + I_E R_E$$

But in the active region $I_E = (\beta + 1) I_B$:

$$V_{BB} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

Now we solve for I_B :

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1) R_E}$$

And multiply both sides by β :

$$\beta I_B = I_C = \frac{\beta (V_{BB} - V_{BE})}{R_B + (\beta + 1) R_E}$$

We complete the analysis with KVL around C-E loop:

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

Bias Stability

Bias stability can be illustrated with equation below:

$$\beta I_B = I_C = \frac{\beta (V_{BB} - V_{BE})}{R_B + (\beta + 1) R_E}$$

Notice that if $R_E = 0$, we have *fixed bias*. While if $R_B = 0$, we have *constant base bias*.

To maximize bias stability:

1. We minimize variations in I_C with changes in β.
   By letting $(\beta + 1) R_E >> R_B$, then β and (β + 1) nearly cancel in above equation

$$\left.\begin{array}{ll} \textit{Rule of Thumb:} & \text{let } (\beta + 1) R_E \approx 10\ R_B \\ \textit{Equivalent Rule:} & \text{let } I_{R_2} \approx 10 I_{B_{max}} \end{array}\right\} \quad \beta = 100$$

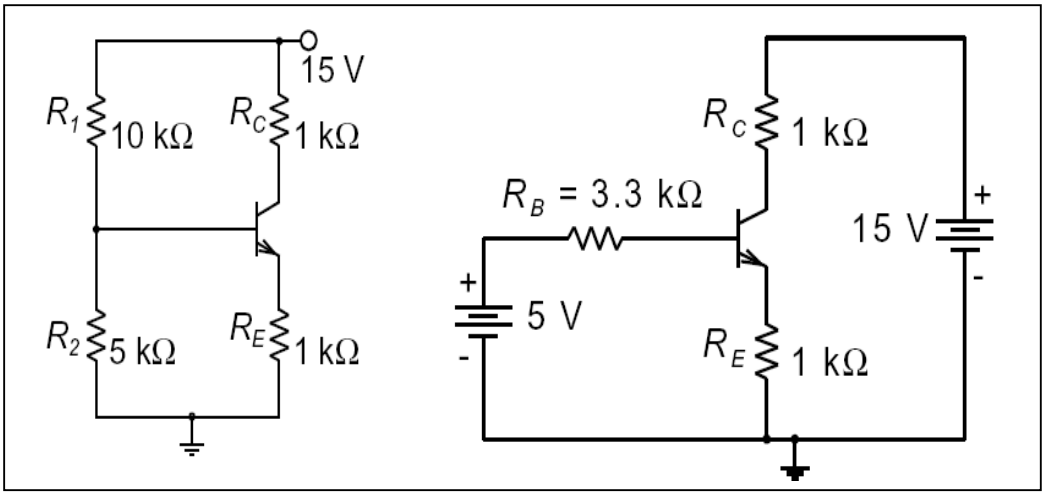
2. We also minimize variations in I_C with changes in V_{BE} . . .
   By letting $V_{BB} >> V_{BE}$

$$\textit{Rule of Thumb:} \qquad \text{let } V_{R_C} \approx V_{CE} \approx V_{R_E} \approx \frac{1}{3} V_{CC}$$

$$\text{Because } V_{R_E} \approx V_{BB} \text{ if } V_{BE} \text{ and } I_B \text{ are small.}$$

Example

For the circuit shown below, determine the stability of the circuit when vary from 100 to 300.



For β = 100 (and V_{BE} = 0.7 V):

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = 41.2\ \mu A \quad \Rightarrow \quad I_C = \beta I_B = 4.12\ mA$$

$$\Rightarrow \quad I_E = \frac{I_C}{\alpha} = 4.16\ mA \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.72\ V$$

For β = 300:

$$I_B = \frac{V_{BB} - V_{BE}}{R_B + (\beta + 1)R_E} = 14.1\ \mu A \quad \Rightarrow \quad I_C = \beta I_B = 4.24\ mA$$

$$\Rightarrow \quad I_E = \frac{I_C}{\alpha} = 4.25\ mA \quad \Rightarrow \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E = 6.50\ V$$

Thus we have achieved a reasonable degree of bias stability.

Procedure

1. Connect the circuit shown in Fig.(4).
2. Change values of "R_B" until I_C=5mA, then record the value of R_B.
3. Connect the source which gives I_{CO}. Then change the voltage source until I_{CO} = 15μA. Record the value of collector current I_C.
4. Repeat step (3) for I_{CO} = (20, 25, 30)μ A.
5. Connect the circuit shown in Fig.(5)
6. Record the value of collector current without I_{CO}.
7. Repeat steps (3, 4) for R_1= kΩ & R_2= kΩ.
8. Repeat steps (6, 7) for R_1= kΩ & R_2= kΩ.

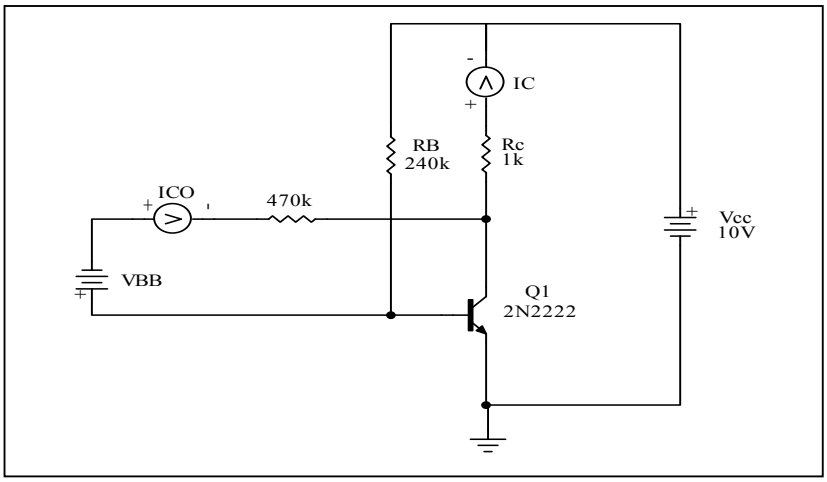


Fig.(4): Fixed Biasing Circuit with I_{CO} source for test

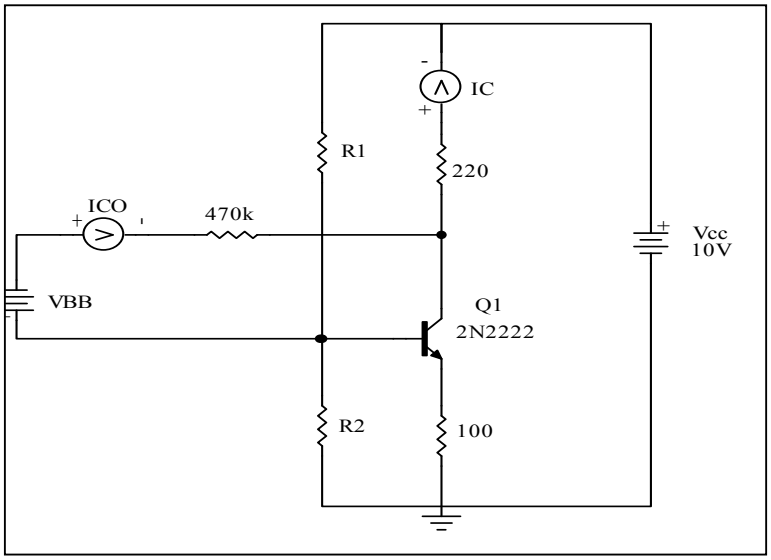


Fig.(5): Self-bias circuit with I_{CO} source for test

Calculations:

1. Plot the relationship between I_C & I_{CO} for two circuits.
2. Find the stability factor for each case.

Discussion

1. What the factors effects on the selection operating point (Q-point).
2. What the effect of decrease the values of R_1 and R_2 on the stability factors. What the disadvantage of using small values of R_1 and R_2.
3. Why we need stable operating point.
4. By using load line and Q-point, explain how the change in I_{CO} effect on the amplifier output.

Experiment No. 9
Two-Port Network & The Hybrid Model

Aim of experiment:

To study the two port network

Theory

The box in the Fig.(1) represents a two-port network which have two voltages and two currents. We may select two of four quantities as the independent variables and express the remaining two in terms of the chosen independent variables.

$$v_1 = h_{11} i_1 + h_{21} v_2$$
$$i_2 = h_{12} i_1 + h_{22} v_2$$

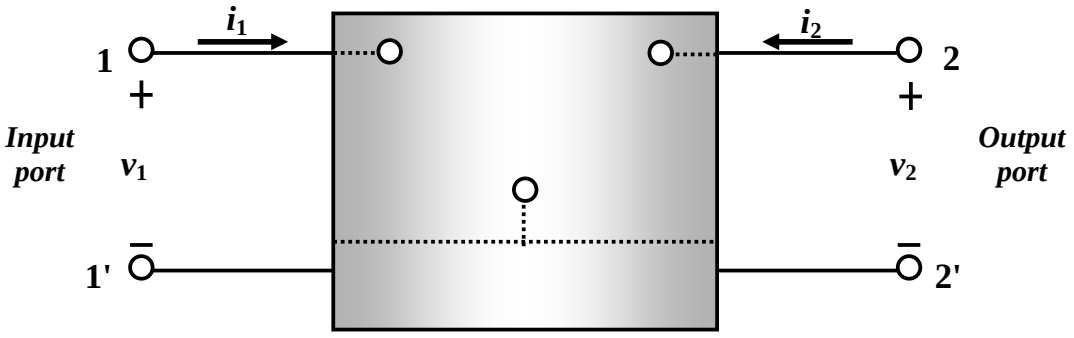


Fig.(1): Two-port network

The quantities h_{11}, h_{12}, h_{21} and h_{22} are called the *h*, or hybrid parameters because they are not all alike dimensionally. Let us assume that there are no reactive elements within the two-port network. Then from above equations, the h parameters are defined as follows:

$h_{11} \equiv \left.\frac{v_1}{i_1}\right|_{v_2=0}$ = input resistance with output short-circuited (ohm)

$h_{12} \equiv \left.\frac{v_1}{v_2}\right|_{i_1=0}$ = fraction of output voltage at the input with input open circuited (dimensionless).

$h_{21} \equiv \left.\frac{i_2}{i_1}\right|_{v_2=0}$ = negative of current transfer ratio or current gain with output short circuited (dimensionless)

$h_{22} \equiv \left.\frac{i_2}{v_2}\right|_{v_1=0}$ = output conductance with input open-circuited (ohm^{-1}).

Notation : The following convenient alternative subscript notation is recommended by the **IEEE Standards**:

***i*=11= input**	***o* = 22 = output**
***f* =21 = forward transfer**	***r* = 12 = reverse transfer**

In the case of transistors, another subscript (b, e, or c) is added to designate the type of configuration. For example,

- $h_{ib} = h_{11b}$ = input resistance in common –base configuration
- $h_{fe} = h_{21e}$ =short- circuit forward current gain in common-emitter circuit.

We may now use the four h parameters to construct a mathematical model of the device of Fig.(1). The hybrid circuit for any device indicated in Fig.(2). We can verify that the model of Fig.(2) satisfies above equations by writing Kirchhoff's voltage and current laws for input and output ports.

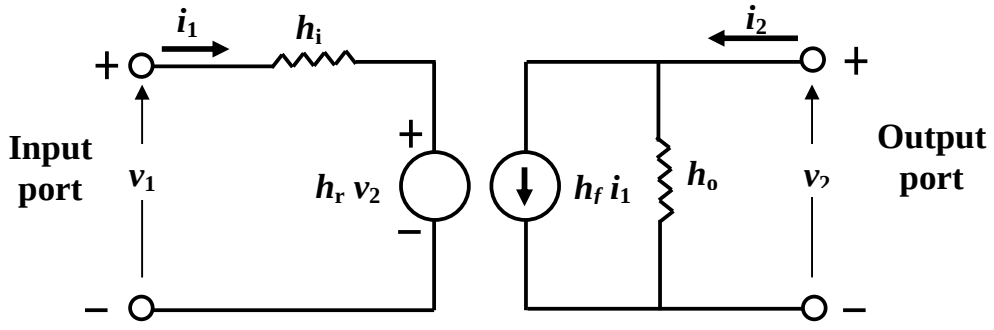


Fig.(2): The hybrid model for two-port network

Procedure

1. Connect the circuit shown in Fig.(3). With output is short-circuited, put v_1=10V and measure i_1, i_2. Then calculate h_{11}, h_{21}.
2. Connect the circuit shown in Fig.(4). With input is open-circuited, put v_2 = 10V and measure v_1, i_2. Then calculate h_{12} and h_{22}.

Discussion:

1. Calculate the theoretical values of h parameters and compare it with result.
2. If you give two-port network with h_{11}=3k□, h_{22}=.2m□$^{-1}$, h_{12}=0.7 and h_{21}= 0.5, find the input voltage to give 1mA pass through the load resistance equal to 1k□.
3. What the deference between the two-port network and two terminals network?
4. Why we used two-port network to analyze the transistor circuit?

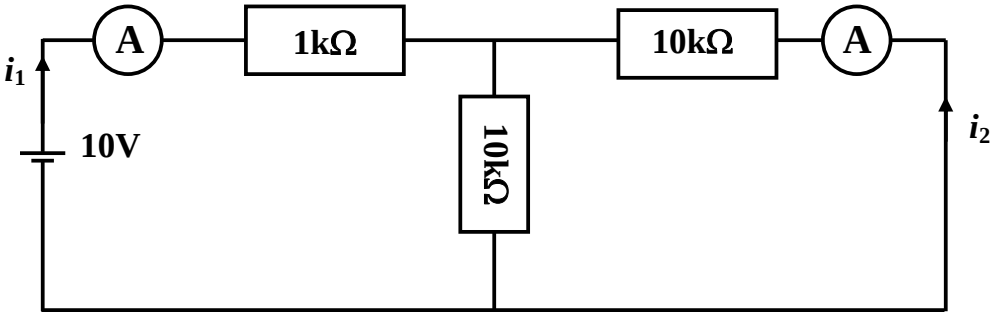


Fig.(3)

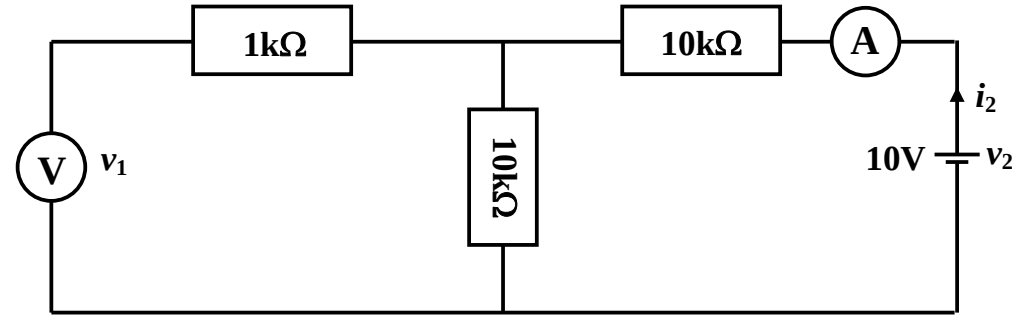


Fig.(4)

Experiment No.4

Zener diode Characteristics

Object:

To study and measure the effects of forward and reverse bias on the zener diode current. To construct a zener voltage regulator and experimentally determine the range over which the zener maintains a constant output voltage.

Theory:

Diodes which are designed with adequate power dissipation capabilities to operate the
break down region may be employed as voltage reference or constant voltage devices such diode are known as avalanche break down of zener diodes.
There are two mechanism which cause reverse break down of diodes, one is called the zener effect and the other the avalanche effect both these effects are due to the large fields
that are set up across the depletion layer when the diode junction is reverse biased, these
fields can become large enough to break electrons away from their covalent bonds and
provide carries for conduction, this is called the zener break down.

Procedure (A):

1. Connect the circuit shown in Figure (l), the power supply is set to zero volts.
2. Measure and record in table (1), the forward current in the diode at each level of voltage (V_f).
3. Determine the forward resistance $R_f = V_f / I_f$.

Procedure (B):

1. Reverse the diode in the circuit of Figure (l).
2. Measure and record in the table (2), the reverse current in the diode at each level of voltage.
3. Calculate $R_z = V_z / I_z$, and record the result in table (2)

Procedure (C):

1. Connect the circuit of Figure (2), the output of the power supply.
2. Slowly increase the supply voltage until E=20V , this voltage must remain constant, change the load resistance and record Vi, Ii , I_z, R_z, in table (3).

Discussion:

1. What is the differences between a normal diode and a zener diode ?
2. Explain how the regulator circuit in Figure (2), works?
3. If you are going to design a regulator circuit , what are the important parameters that should know about the zener ?

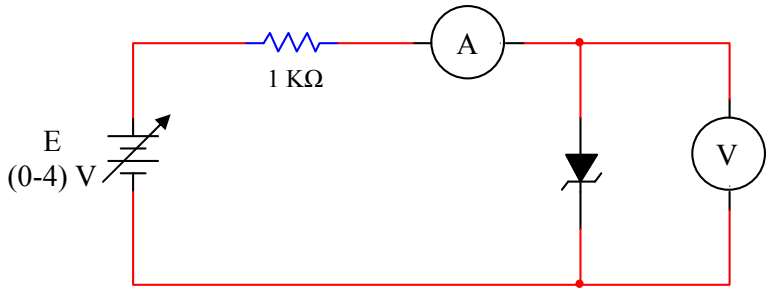


Figure (1)

V_f	0	0.1	0.2	0.3	0.4	0.5	0.6	0.7
I_f								
R_f								

Table (1)

V_Z	0	2	4	5	7	10	12	13	14	15.1
I_Z										
R_Z										

Table (2)

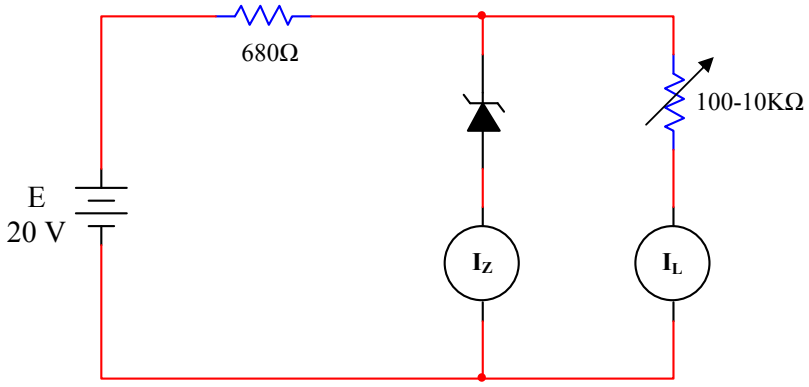


Figure (2)

E (v)	R_L (Ω)	V_L (v)	I_L (mA)	I_Z (mA)
20	200 400 600 800 1 K 1.5 K 2 K 4 K 6 K 8 K 10 K			

Table (3)