Design and Implementation of a High Resolution Two Counter Digital Pulse Width Modulation

Abstract

This paper presents a high resolution Digital Pulse Width Modulation "DPWM" for thevoltage regulator application. The PWM signal is generated by using two fast clockcounters. In this approach, the pulse width is combined from two parts depending on twocounter schemes. MSBs of the DPWM generates first part of pulse that achieved by a firstcounter-phase comparator scheme, and the LSBs of the DPWM generates second part ofpulse that obtained through a second counter- phase comparator scheme. The resolution ofpresent pulse width depends on the resolution of second counter.The developed pulse width modulator has high precision, good linearity, and wide dutycycle range. Further, it can be flexibly reconfigured for multi-phase PWM operation with norestriction on duty cycle range. In this work, a 714 kHz switching frequency DPWM modulewith 9- bit resolution is tested by simulation program