Microprocessor 8085

The 8085 MPU:

We define the MPU as a device or a group of devices (as a unit) that can communicate with peripherals. Provide timing signals, direct data flow, and perform computing tasks as specified by the instructions in memory.

Using this description, the 8085 microprocessor can almost qualify as an MPU, but with the following two limitations:

1. The low – order address bus of the 8085 microprocessor is multiplexed (time shared) with the data bus. The buses need to be demultiplexed.
2. Appropriate control signals need to be generated to interface memory and I/O with the 8085.

(Intel has some specialized memory and I/O devices that don't require such control signals).

The 8085 Microprocessor:

All the signals can be classified into six groups: (as shown in figure 1)

1. Address bus.
2. Data bus.
3. Control and status signals.
4. Power supply and frequency signals.
5. Interrupts and peripheral initiated signals.
6. Serial I/O signals.

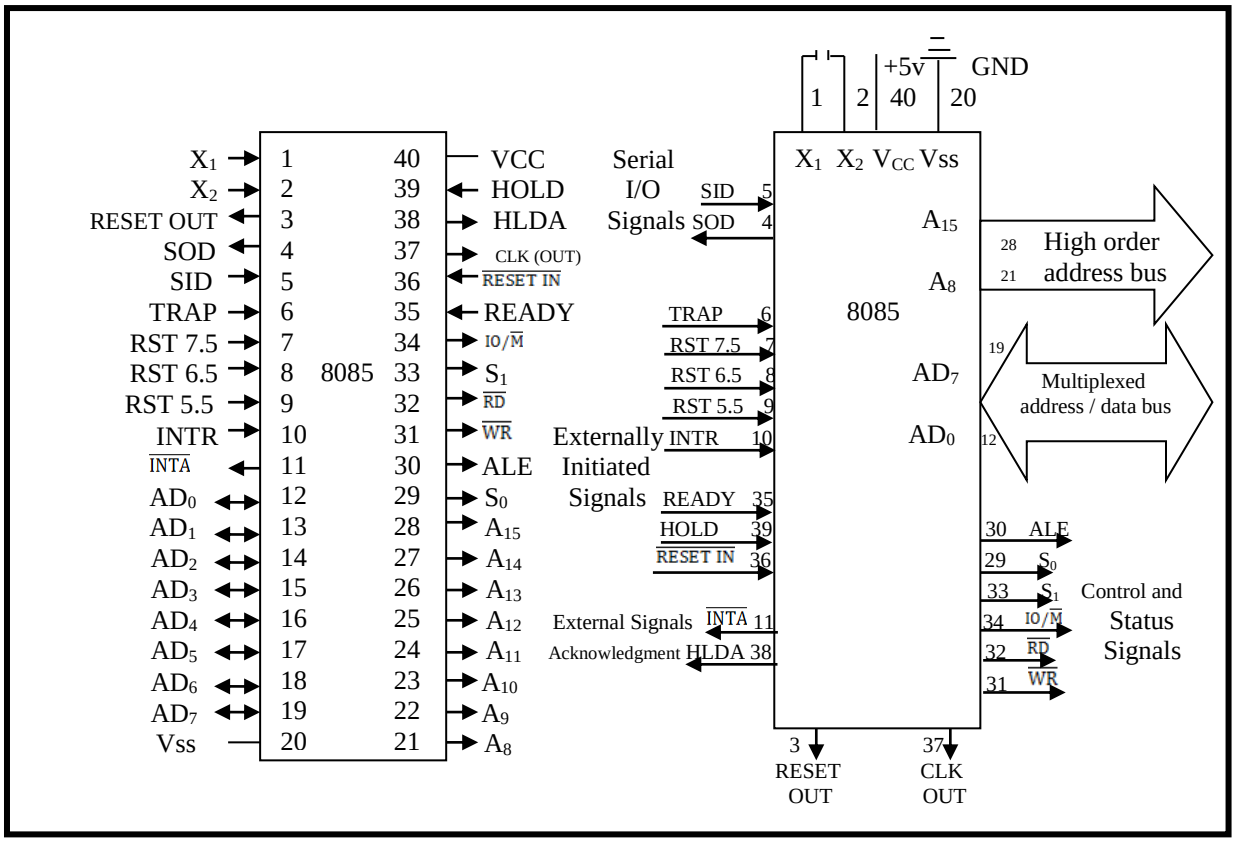

Figure 1: Microprocessor 8085 pin configuration

1. Address bus:

The 8085 has eight signal lines, $A_{15} – A_8$, which are unidirectional and used as the high–order address bus.

2. Multiplexed address / data bus:

The signal lines AD_7 to AD_0 are bidirectional, they serve a dual purpose.

They are used as the low – order address bus as well as the data bus.

In executing an instruction, during the earlier part of the cycle, these lines are used as the low – order address bus.

During the later part of the cycle, these lines are used as the data bus.

(This is also known as multiplexing the bus.) However, the low – order address bus can be separated from these signals by using a latch.

3. Control and status signals:

This group of signals includes two control signals (RD and WR), three status signals (IO/M, S_1 and S_0) to identify the nature of the operation.

And one special signal (ALE) to indicate the beginning of the operation.

These signals are as follows:

A. ALE – Address Latch Enable:

This is a positive going pulse generated every time the 8085 begins an operation (machine cycle): it indicates that the bits on $AD_7 - AD_0$ are address bits.

This signal is used primarily to latch the low – order address from the multiplexed bus and generate a separate set of eight address lines, A_7 to A_0.

B. RD – Read:

This is a read control signal (active low). This signal indicates that the selected I/O or memory device is to be read and data are available on the data bus.

C. WR – Write:

This is a write control signal (active low). This signal indicates that the data on the data bus are to be written into a selected memory or I/O location.

D. IO/M:

This is a status signal used to differentiate between I/O and memory operations.

When it is high, it indicates an I/O operation.

When it is low, it indicates a memory operation.

This signal is combined with RD (Read) and WR (Write) to generate I/O and memory control signals.

E. S_1 and S_0:

These status signals similar to IO/M, can identify various operations, but they are rarely used in small systems.

4. Power supply and clock frequency signals:

The power supply and frequency signals are as follows.

*Vcc: +5 volt power supply.

*Vss: Ground Reference.

*X_1, X_2: A crystal (or RC, LC network) is connected at these two pins.

The frequency is internally divided by two; therefore, to operate a system at 3MHz, the crystal should have frequency of 6 MHz

*CLK (OUT) – Clock Output: This signal can be used as the system clock for other devices.

5. Interrupts and peripheral initiated signals:

The 8085 has five interrupt signals that can be used to interrupt a program execution.

One of the signals, INTR (Interrupt Request), is identical to the 8085A microprocessor interrupt signal (INT); the others are enhancements to 8085A.

The microprocessor acknowledges an interrupt by the INTA (Interrupt Acknowledge) signal.

In addition to the interrupts, these pins – RESET, HOLD, and READY – accept the externally initiated signals as inputs.

To respond to the HOLD request, it has one signal called HLDA (Hold Acknowledge).

The RESET is described below:

*RESET IN:

When the signal on this pin goes low, the program counter is set to zero.

The buses are tri – stated, and the MPU is reset.

*RESET OUT:

This signal indicates that the MPU is being reset. The signal can be used to reset other devices.

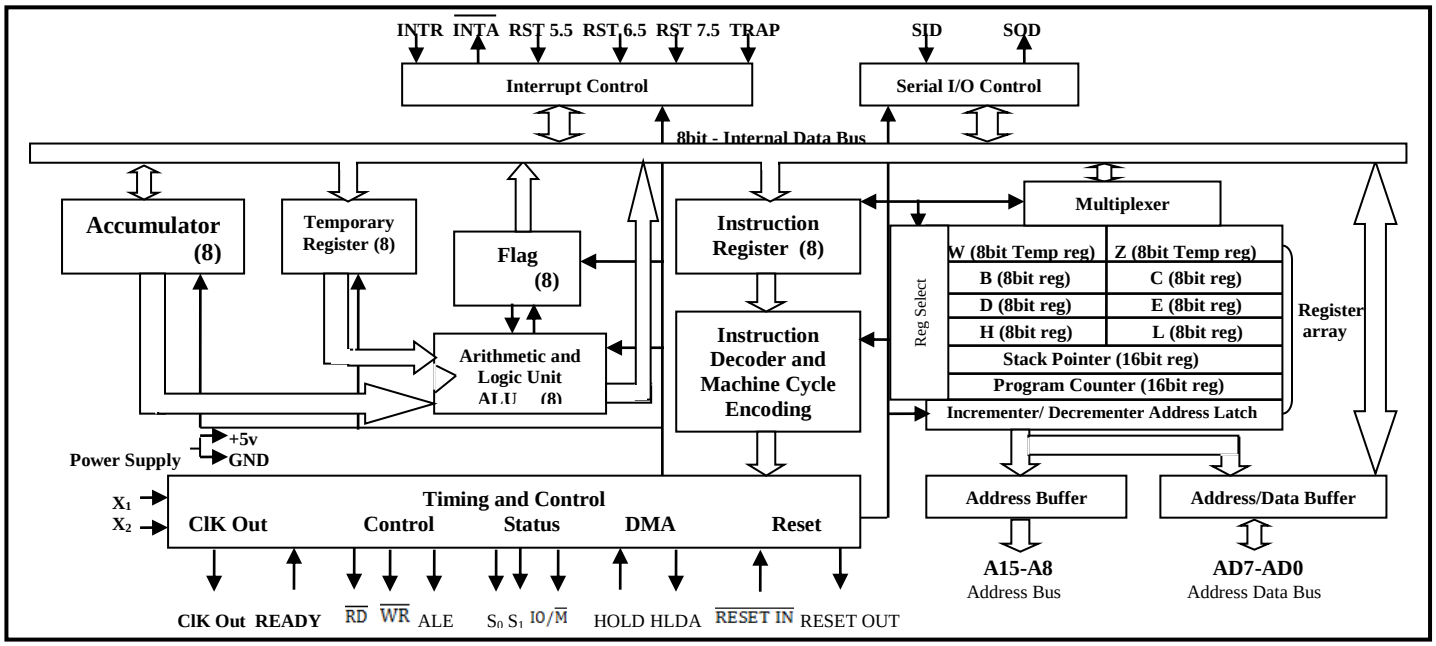

Figure 2: Microprocessor 8085 Function block diagram

6. Serial I/O signals:

The 8085 has two signals to implement the serial transmission: SID (Serial Input Data) and SOD (Serial Output Data).