PROGRAMMED TIME DELAYS

OBJECTIVES:

- Compute the time required to execute an 8085 assembly language program.
- Design nested delay loops to generate a precise delay time.
- Generate a repetitive digital signal having a precise frequency.

INTRODUCTION

Each 8085 instruction requires a specific amount of execution time. In most applications, the programmer will attempt to minimize this execution time by writing the program in an efficient manner. There are many situations however, in which desirable to generate a time delay. This delay time can serve as a time to generate periodic waveforms or to sequence an industrial process.

The execution time required by each instruction is function of the number of (T-states) in its instruction cycle. Each T-state is equal to one period of the 8085 system clock. For example, if an 8085 microprocessor has a clock frequency of 2 MHz, then each T-state equal 0.5 µs. assuming this clock frequency, the instruction MVI A,byte, which consumes seven T-states, would be executed in

Clock frequency of the system f=2MHZ
Clock period T=1/f= 1/2 *10^{-6}=0.5 µs /T-states
Time to execute MVI=7 T-states*0.5µs / T-states =3.5 µs
Note:- Compute the same calculation when clock frequency=3.125MHZ, then each T-state equal 320ns.

The time delay generated by a program is compounded by nesting loops within other loops. The total delay will then be the product of the individual delay for each loop. If longer loops are required, register pairs may be used for loop counters. Statements such as XTHL are often placed inside delay loops as "padding", to increase the total delay time.

- Note: INX rp and DCX rp instruction do not modify the Z flag. In other words, a JZ or JNZ instruction immediately following a DCX rp or INX rp instruction is not satisfactory, and an arithmetic or logic operation must be executed first.

Useful instructions:

NOP: No operation is performed. The instruction is fetched and decoded; however, no operation is executed. The instruction is used to fill in time delays and insert instructions while troubleshooting.

Instruction	Type	No. of Bytes	Function	Effect
NOP	Machine control	1	No operation	None

Example:-

		T-states
	MVI C,0FFh	7
Loop:	DCR C	5
	JNZ loop	10

In this example, register C is loaded with the count ff (255) by the instruction MVI, which is executed once and takes seven T-states. The next two instructions, DCR and JNZ, from a loop with a total of fifteen (5+10) T-states. The loop is repeated 255 times until C=0. The time delay in the loop T_L with 2 MHZ clock frequency is calculated as:-

T_L= (T* loop T-states * N_{10})

Where T_L : Time delay in the loop

T: system clock period

N_{10}: equivalent decimal number of the hexadecimal count loaded in the delay register.

=($0.5*_{10}^{-6}$ *15*255)

= 1912.5µs

However, to calculate the time delay more accurately, the time for the execution of the initial instruction MVI should be included in the total time delay T_D as:

Delay T_D = Time to execute instructions outside loop + time to execute loop instructions

= T_0+ T_L

= (7*0.5µs) + 1912.5µs

= 1916µs