Introduction to semiconductor

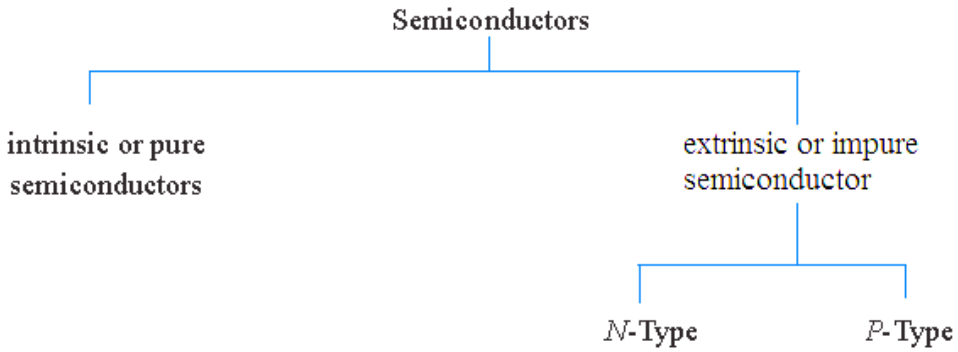
Semiconductors:

A semiconductor material is one whose electrical properties lie in between those of insulators and good conductors. Examples are: germanium and silicon.

In terms of energy bands, semiconductors can be defined as those materials which have almost an empty conduction band and almost filled valence band with a very narrow energy gap (of the order of 1 eV) separating the two.

Types of Semiconductors:

Semiconductor may be classified as under:



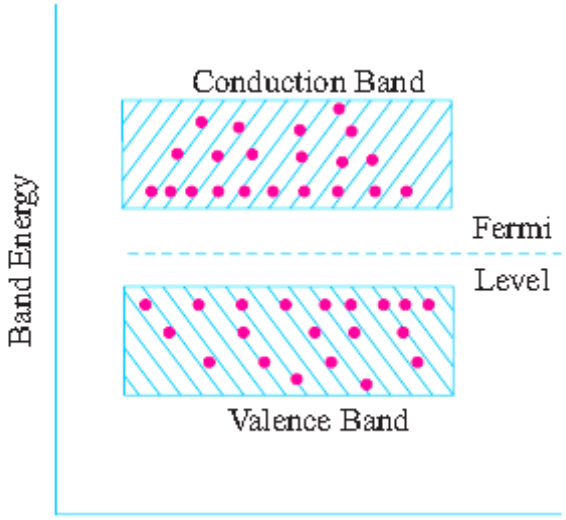
a. Intrinsic Semiconductors

An intrinsic semiconductor is one which is made of the semiconductor material in its extremely pure form.

Examples of such semiconductors are: pure germanium and silicon which have forbidden energy gaps of 0.72 eV and 1.1 eV respectively. The energy gap is so small that even at ordinary room temperature; there are many electrons which possess sufficient energy to jump across the small energy gap between the valence and the conduction bands.

Alternatively, an intrinsic semiconductor may be defined as one in which the number of conduction electrons is equal to the number of holes.

Schematic energy band diagram of an intrinsic semiconductor at room temperature is shown in Fig. below.



b. <u>Extrinsic Semiconductors:</u>

Those intrinsic semiconductors to which some suitable impurity or doping agent or doping has been added in extremely small amounts (about 1 part in 10^8) are called extrinsic or impurity semiconductors.

Depending on the type of doping material used, extrinsic semiconductors can be sub-divided into two classes:

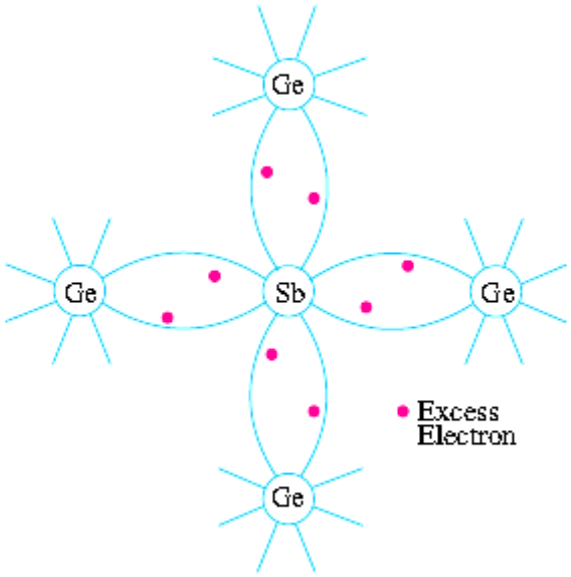
(i) N-type semiconductors and

(ii) P-type semiconductors.

(i) N-type Extrinsic Semiconductor:

This type of semiconductor is obtained when a pentavalent material like antimonty (Sb) is added to pure germanium crystal. As shown in Fig. below, each antimony atom forms covalent bonds with the surrounding four germanium atoms with the help of four of its five electrons. The fifth electron is superfluous and is loosely bound to the antimony atom.

Hence, it can be easily excited from the valence band to the conduction band by the application of electric field or increase in thermal energy. It is seen from the above description that in N-type semiconductors, electrons are the majority carriers while holes constitute the minority carriers.

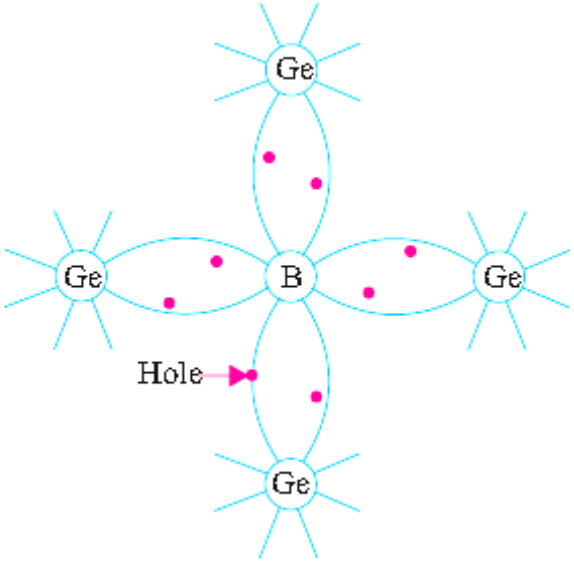


(ii) P-type Extrinsic Semiconductor:

This type of semiconductor is obtained when traces of a trivalent like boron (B) are added to a pure germanium crystal. In this case, the three valence electrons of boron atom form covalent bonds with four surrounding germanium atoms but one bond is left incomplete and gives rise to a hole as shown in Fig. below.

Thus, boron which is called an acceptor impurity causes as many positive holes in a germanium crystal as there are boron atoms thereby producing a P-type (P for positive) extrinsic semiconductor.

In this type of semiconductor, conduction is by the movement of holes in the valence band.



Majority and Minority Carriers:

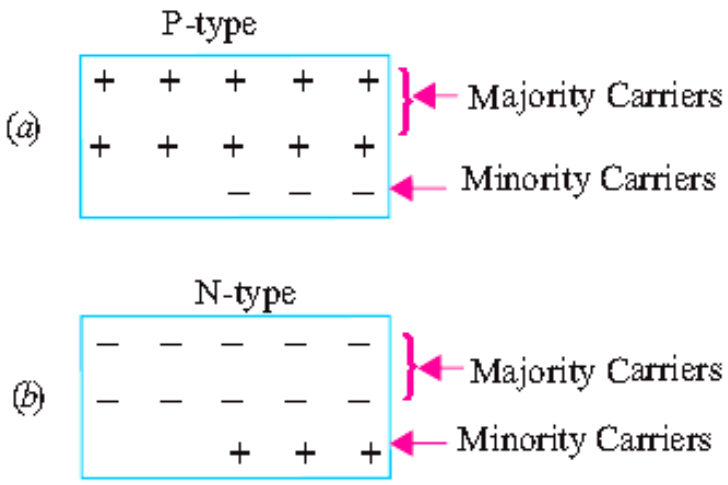
In a piece of pure germanium or silicon, no free charge carriers are available at 0^oK. However, as its temperature is raised to room temperature, some of the covalent bonds are broken by heat energy and as a result, electron-hole pairs are

Produced. These are called thermally-generated charge carriers. They are also known as intrinsically-available charge carriers. Ordinarily, their number is quite small. An intrinsic of pure germanium can be converted into a P-type semiconductor by the addition of an acceptor impurity which adds a large number of holes to it. Hence, a P-type material contains following charge carriers:

(a) Large number of positive holes—most of them being the added impurity holes with only a very small number of thermally generated ones.

(b) A very small number of thermally-generated electrons (the companions of the thermally generated holes mentioned above).

Obviously, in a P-type material, the number of holes (both added and thermally-generated) is much more than that of electrons. Hence, in such a material, holes constitute majority carriers and electrons form minority carriers as shown in Fig. below (a). Similarly, in an N-type material, the number of electrons (both added and thermally-generated) is much larger than the number of thermally-generated holes. Hence, in such a material, electrons are majority carriers whereas holes are minority carriers as shown in Fig. below (b).



P-N Junction Diode

1. Construction

It is two terminal devices consisting of a P-N junction formed either in Ge or Si crystal. It is circuit symbol is shown in fig. (1-a). The P and N type regions are referred to as anode and cathode respectively. In fig. (1-b) arrowhead indicates the conventional direction of current flow when forward biased. It is the same direction in which hole flow takes place.

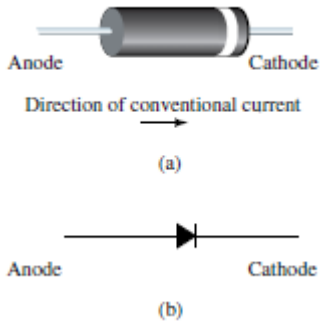


Fig.1

2. Working

A P-N junction diode is a one way device offering low resistance when forward biased and behaving almost as an insulator when reverse biased. Hence such diodes are mostly used as rectifiers for converting alternating current into direct current.

3. V/I Characteristic

Fig.2 shows the static voltage current characteristics for a low power P-N junction diode.

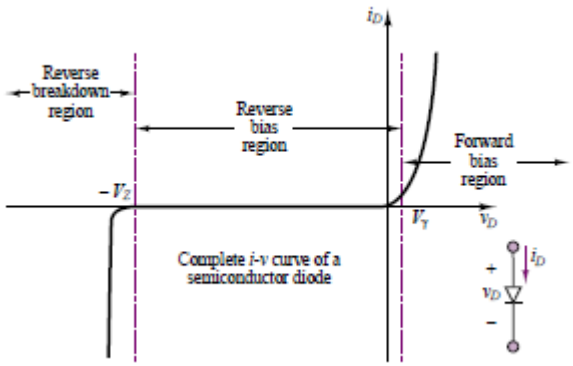


Fig. 2

3.1 Forward characteristic

When the diode is forward biased and applied voltage is increased from zero hardly any current flows through the device in the beginning. It is so because the external voltage is being opposed by the internal barrier voltage V_B whose value is 0.7 V for Si and 0.3 V for Ge. As soon as V_B is neutralized, current through the diode increases rapidly with increasing applied battery voltage. It is found that as little a voltage as 1.0 V produces a forward current of about 50 mA.

3.2 Reverse characteristic

When the diode is reverse biased majority carriers are blocked and only a small current (due to minority carriers) flows through the diode. As the reverse voltage is increased from zero, the reverse current very quickly reaches its maximum or saturation value I_0 which is also known as leakage current. It is of order of nano ampers (nA) for Si and micro ampers (µA) for Ge. As seen from fig.2 when reverse voltage V_{BR}, the leakage current

suddenly and sharply increases, the curve indicating zero resistance at this point.

4. Diode Parameters

4.1 Bulk resistance (r_B)

It is the sum of the resistance values of the P and N type semiconductor materials of which the diode is made of

$$r_B = r_P + r_N$$

Usually, it is very small, it is given by

$$r_B = \frac{V - V_K}{I_F}$$

It is the resistance offered by the diode well above the knee voltage when current resistance is large.

Obviously, this resistance is offered in the forward direction.

4.2 Junction resistance (r_j)

It is value for forward biased junction depends on the magnitude of forward dc current.

$$r_j = \frac{25\ mV}{I_F mA} \ldots\ldots\ldots\ldots\ for\ Ge$$

$$r_j = \frac{50\ mV}{I_F\ mA} \ldots\ldots\ldots\ldots\ for\ Si$$

4.3 Dynamic or ac resistance

$$r_{ac} \text{ or } r_d = r_B + r_j$$

For large values of forward current, r_j is negligible. Hence, $r_{ac} = r_B$ for small values of I_F, r_B is negligible as compared to r_j

$$r_{ac} = r_j$$

4.4 Forward voltage drop

It is given by the relation

$$forward\ voltage\ drop = \frac{power\ dissipated}{forward\ dc\ current}$$

Reverse saturation current (I_0)

Reverse breakdown voltage (V_{BR})

Reverse dc resistance (R_R)

$$R_R = \frac{reverse\ voltage}{reverse\ current}$$

5. Equation of diode current

The analytical equation which describes both the forward and reverse characteristics is called the Boltzmann's diode equation given

$$I = I_0(e^{40V} - 1) \ldots\ldots\ldots for\ Ge$$

$$I = I_0 e^{40V} \quad if\ V > 1\ volt.$$

$$\text{And } I = I_0(e^{20V} - 1) \ldots\ldots\ldots for\ Si$$

$$I = I_0 e^{20V} \quad if\ V > 1\ volt.$$

Where I_0 reverse saturation current. V voltage across the diode.

Rectifier:

It is a circuit which employs one or more diodes to convert ac voltage into pulsating dc voltage.

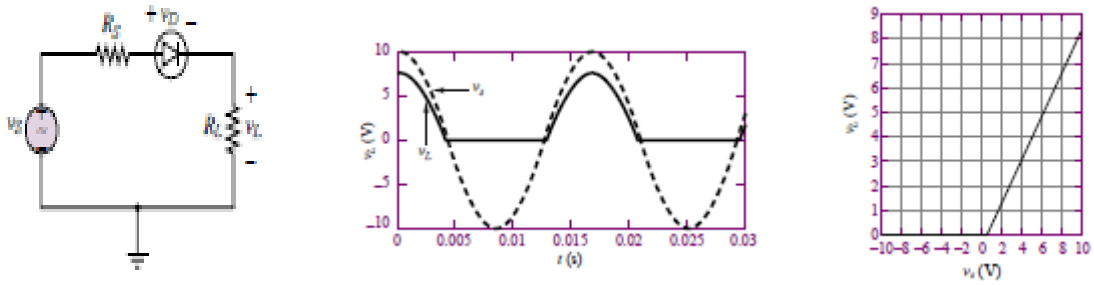
We will consider the following circuits:

(i) Half wave rectifier.
(ii) Full wave rectifier.
(iii) Full wave bridge circuits.
(iv) Voltage multiplier circuits.

Half wave rectifier

Basic half wave rectifier circuit is shown in fig.1 along with its input and output waveforms. An alternating voltage is applied to a single diode connected in a series with a load resistor R_L.

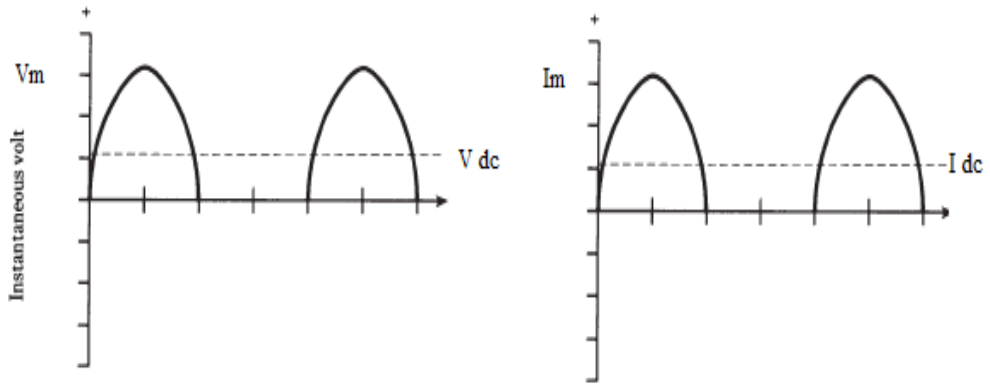
Working: during the positive half cycle of the input ac voltage the diode D is forward biased (ON) and conducts while conducting the diode acts as a short circuit so that circuit current flows and hence, positive half cycle of the input ac voltage is dropped across R_L.



During the negative half cycle, the diode is reversing biased (off), and so does not conduct. There is no current flow, hence there is no voltage drop across R_L, I_D=0 and V_L=0.

Average values

We will now state the average values of the output voltage and current. These are showing in fig.2.



Let the equation of the input supply voltage of fig.1 be

$V = V_m \sin\theta$

V_m= maximum value of supply voltage in fig.1

$=\sqrt{2}V$

V= rms value of supply voltage.

I_m= maximum value of diode or load current.

V_{dc}= average dc voltage across load.

I_{dc}= average dc current through load.

I_{rms}= rms current through load.

Then it can be proved that

(i) $V_{dc} = \frac{V_m}{\pi} = 0.318\, V_m$

(ii) $I_{dc} = \frac{V_{dc}}{R_L} = \frac{V_m}{\pi R_L}$

$= 0.318 \frac{V_m}{R_L}$

$= 0.318\, I_m$

$= 0.45\, \frac{V}{R_L}$

$I_{rms} = \frac{I_m}{2} = 0.5\, I_m$

(iii) Form Factor

$$F = \frac{rms\ value}{average\ value} = \frac{0.5\, I_m}{0.318\, I_m} = 1.57\ \ for\ sinusoidal\ ac\ wave$$

(iv) PIV

It is the maximum voltage across the diode in the reverse direction.

(v) Ripple Factor (γ)

The ripple factor of a single phase half wave rectifier is

$$\gamma = \frac{V_{rms}}{V_{dc}}$$

$$= \frac{0.385\, V_m}{0.318\, V_m} = 1.21$$

The relation between V_m and V_{dc} is given by

$$\frac{V_m}{V_{dc}} = 1 + \sqrt{3}.\gamma$$

(vi) Efficiency (η)

It is given by the ratio of the output dc power to the total amount of input power supplied to the circuit

$$\therefore \eta = \frac{P_{out}}{P_{in}}$$

$$now, P_{out} = I_{dc}^2 R_L$$

$$P_{in} = I_{rms}^2 (r_d + R_L)$$

$$\therefore \eta = \frac{I_{dc}^2 R_L}{I_{rms}(r_d + R_L)} \times 100$$

$$substituting\ and\ simplifying\ we\ get$$

$$\eta = \frac{0.406}{1 + \frac{r_d}{R_L}}$$

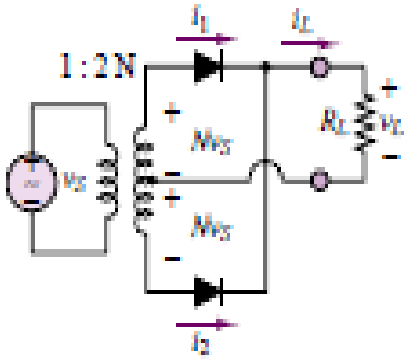
$$= \frac{40.6}{1 + \frac{r_d}{R_L}} \quad percent$$

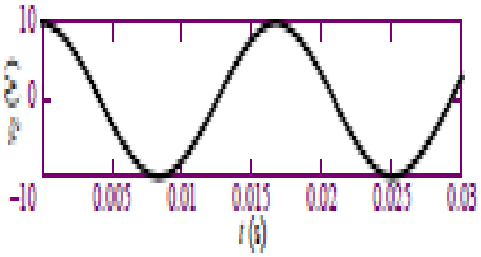
If diode resistance r_d is neglected, then

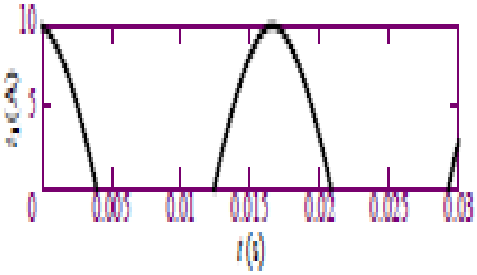
$$\eta = 40.6\,\% \qquad it\ is\ the\ maximum\ possible\ efficiency.$$

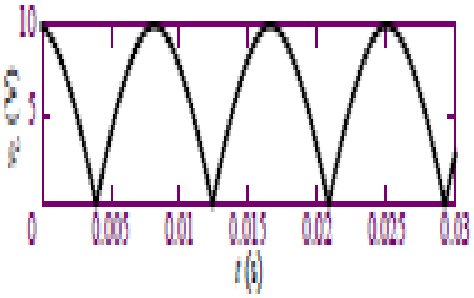
Full -wave Rectifier

The full wave rectifier circuit using two diodes and a center tapped transformer is shown in fig.3. The centers tap. is usually taken as the ground or zero voltage reference point.









(a) Working:

When input ac supply is switched on, the ends of the transformer secondary become +Ve and negative alternately. During the positive half cycle of the ac input. Hence, being forward biased diode D_1 conducts (but not D_2 which is reverse biased). As a result, positive half cycle of the voltage appears across R_L. In the negative half cycle D_2 conducts (but not D_1). So we find that current keeps of following through R_L in the same direction in both half cycles of the ac input. Also, the frequency of the rectified output voltage is twice the supply frequency.

(b) Average values:

(i) $V_{dc} = \frac{2V_m}{\pi}$

$= 0.636\, V_m$ *twice the half wave recifier value*

$= \frac{2\sqrt{2}V}{\pi} = 0.9\, V$

Where V_m is the maximum voltage across each half of the secondary winding.

$V = \frac{V_m}{\sqrt{2}}$

=rms voltage across each half of the secondary winding.

(ii) $I_{dc} = \frac{2I_m}{\pi} = \frac{2}{\pi}\,\frac{V_m}{R_L}$

$= 0.636\, I_m$

$$= \frac{V_{dc}}{R} = \frac{2.\sqrt{2}}{\pi} . \frac{V}{R_L}$$

$$= 0.9 \frac{V}{R_L}$$

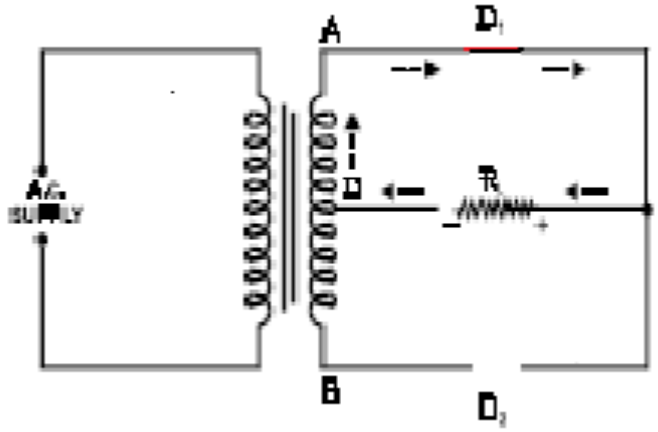
(iii) $I_{rms} = 0.707\, I_m$

(iv) $form\ factor, F = \frac{I_{rms}}{I_{av}} = \frac{I_{rms}}{I_{dc}}$

$$= \frac{0.707\, I_m}{0.636\, I_m} = 1.11$$

(c) PIV:

In this case, PIV rating of each diode is 2 V_m. consider the positive half cycle of the input ac supply when D_1 acts as short and D_2 acts as open since it is reverse biased. A voltage V_m develops across R_L. As seen from fig. below, voltage across D_2 is equal to the sum of voltages across the lower half GN of the transformer secondary and the load resistor. Hence PIV of D_2=2 V_m.



(d) Ripple factor (γ):

For full wave rectifier circuit $\gamma = \frac{V_r(rms)}{V_{dc}} = \frac{0.305\,V_m}{0.636\,V_m} = 0.482$

Is much less than that of half wave rectifier. The relation between V_m and V_{dc} is the same as HW rectifier.

(e) Efficiency:

$$\eta = \frac{P_{out}}{P_{in}}$$

$$= \frac{{I_{dc}}^2 * R_L}{{I_{rms}}^2 (r_d + R_L)}$$

Substituting and simplifying, we get

$$\eta = \frac{81.2\%}{1 + \frac{r_d}{R_L}} = 81.2\% \quad if\ r_d = 0$$

It is twice the value for half wave rectifier.

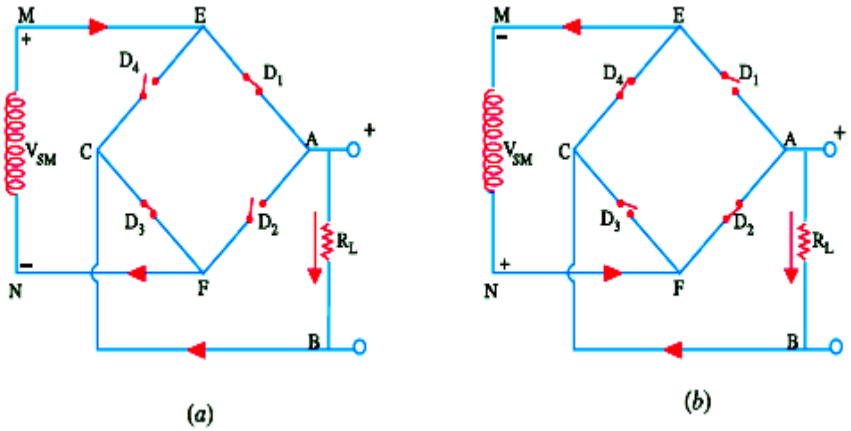
Full-Wave Bridge Rectifier

It is the most frequently-used circuit for electronic dc power supplies. It requires four diodes but the transformer used is not centre-tapped and has a maximum voltage of Vsm.

(*a*) Working

During the positive input half-cycle, terminal *M* of the secondary is positive and *N* is negative as shown separately in Fig. below (*a*). Diodes *D*1 and *D*3 become forward-biased (ON) whereas *D*2 and *D*4 are reverse-biased (OFF). Hence, current flows along *MEABCFN* producing a drop across *RL*.

During the negative input half-cycle, secondary terminal *N* becomes positive and *M* negative. Now, *D*2 and *D*4 are forward-biased. Circuit current flows along *NFABCEM* as shown in Fig. below (*b*). The current keeps flowing through load resistance *RL* in the same direction *AB* during both half-cycles of the ac input supply. Consequently, point *A* of the bridge rectifier always acts as an anode and point *C* as cathode.



(*b*) Average and RMS Values

(i) $V_{dc} = 0.636\, V_m$

$= 0.9V$

$(ii)\quad I_{dc} = \frac{2}{\pi}\frac{V_m}{R_L}$

$= 0.636\, I_m$

$= 0.9 \times \frac{V}{R_L} = 0.9\, I_{rms}$

$(iii)\quad I_{rms} = 0.707\, I_m$

$(iv)\quad form\ factor, F = \frac{I_{rms}}{I_{av}} = \frac{I_{rms}}{I_{dc}}$

$= 1.11$

(c) PIV:

In a full wave bridge rectifier, the PIV rating of each of the four diodes is V_m (not $2V_m$ as the case for ordinary full wave rectifier).

(d) Ripple factor (γ):

It is the same of for ordinary full wave rectifier

$$\gamma = 0.482$$

(e) Efficiency:

It is the same of for ordinary full wave rectifier

$\eta = 81.2\%.$ *if diode resistance is neglected.*

(*f*) Advantages:

1. No centre-tap is required on the transformer.
2. Much smaller transformers are required.
3. It is suitable for high-voltage applications.
4. It has less *PIV* rating per diode.

The obvious disadvantage is the need for twice as many diodes as for the centre-tapped transformer version.

Diode Applications

Diode Clipper and Clamper Circuits

These are diode wave-shaping circuits *i.e*. circuits meant to control the shape of the voltage and current waveforms to suit various purposes. Each performs the wave-shaping function indicated by its name. The output of the clipping circuit appears as if a portion of the input signal were clipped off. But clamper circuits simply lams (*i.e*. lift up or down) the input signal to a different dc level.

Clippers

A clipping circuit requires a minimum of two components *i.e*. a diode and a resistor. Often, dc battery is also used to fix the clipping level. The input waveform can be clipped at different levels by simply changing the battery voltage and by

interchanging the position of various elements. We will use an ideal diode which acts like a closed switch when forward-biased and as an open switch when reverse-biased.

Such circuits are used in radars and digital computers etc. when it is desired to remove signal voltages above or below a specified voltage level. Another application is in radio receivers for communication circuits where noise pulses that rise well above the signal amplitude are clipped down to the desired level.

Example:

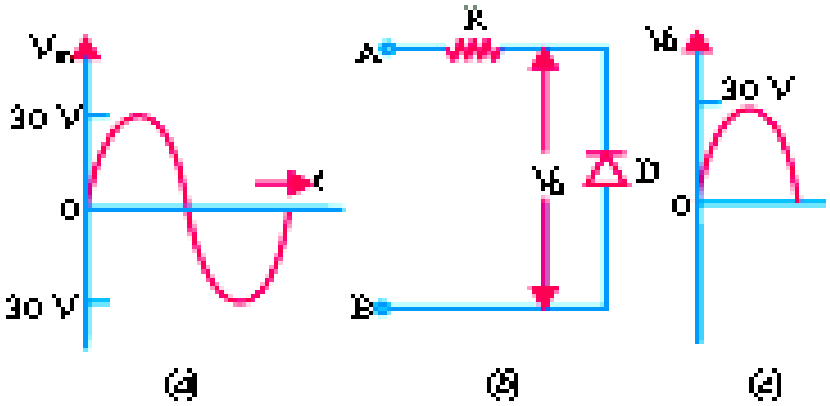
For the simple parallel clipper of Fig. below, find the shape of the output voltage. What will happen when diode and resistor are inter-changed?

Solution:

When positive half-cycle of the signal voltage is applied to the clipper *i.e*. when *A* is positive with respect to *B*, the diode *D* is reverse-biased. Hence, it acts as an open switch. Consequently, the entire input voltage appears across it.

During the negative half-cycle of the signal voltage when circuit terminal *B* becomes positive with respect to *A*, the diode is forward-biased. Hence, it acts like a closed switch (or short) across which no voltage is dropped.

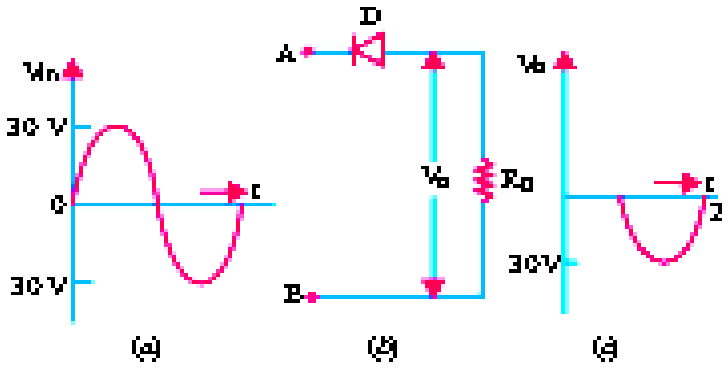
Hence, the wave-shape of V_0 is as shown in Fig. below (*c*). It is seen that the negative portion of the signal voltage has been removed. Hence, such a circuit is called a **negative clipper**.



When Diode and Resistor are Interchanged

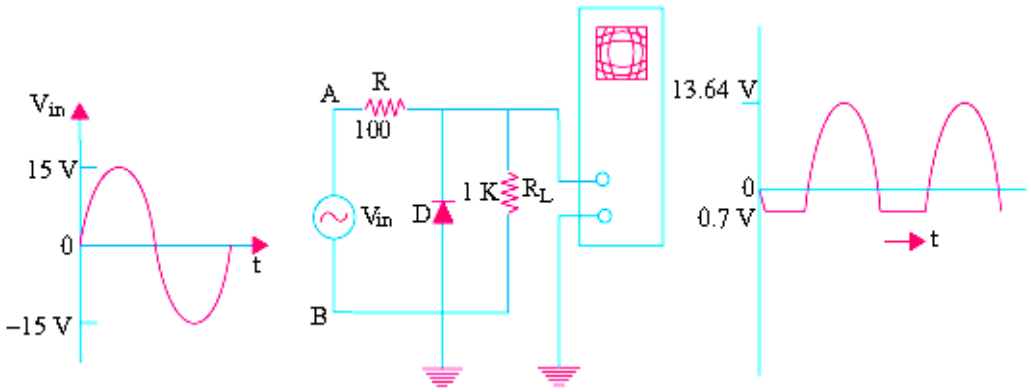
In this case, the circuit becomes as shown in Fig. below. Now, the output voltage *V*0 is that which is dropped across *R*. During the positive half-cycle of the signal voltage, *D* acts as an open switch. Hence, all applied voltage drops across *D* and none across *R*. So, there is no output signal voltage.

During the negative input half cycle, terminal *B* is positive and so it is forward-biases *B* which acts as a short. Hence, there is no voltage drop across *D*. Consequently, all the applied signal voltage drops across *R* and none across *D*. As a result, the negative half-cycle of the input signal is allowed to pass through the clipper circuit. Obviously, now the circuit acts as a **positive clipper.**



Example:

What would be the output waveform displayed by the oscilloscope in Fig. below? The silicon diode has a barrier voltage of 0.7 V.



Solution:

Consider the negative input half-cycle first *i.e*. when point *B* is positive with respect to point *A*. The diode starts conducting when applied voltage exceeds 0.7 V. Since *D* and *RL* are in parallel, voltage across them cannot exceed 0.7 V. Obviously, negative half-cycle beyond 0.7 V gets clipped. Hence, circuit behaves like a negative clipper.

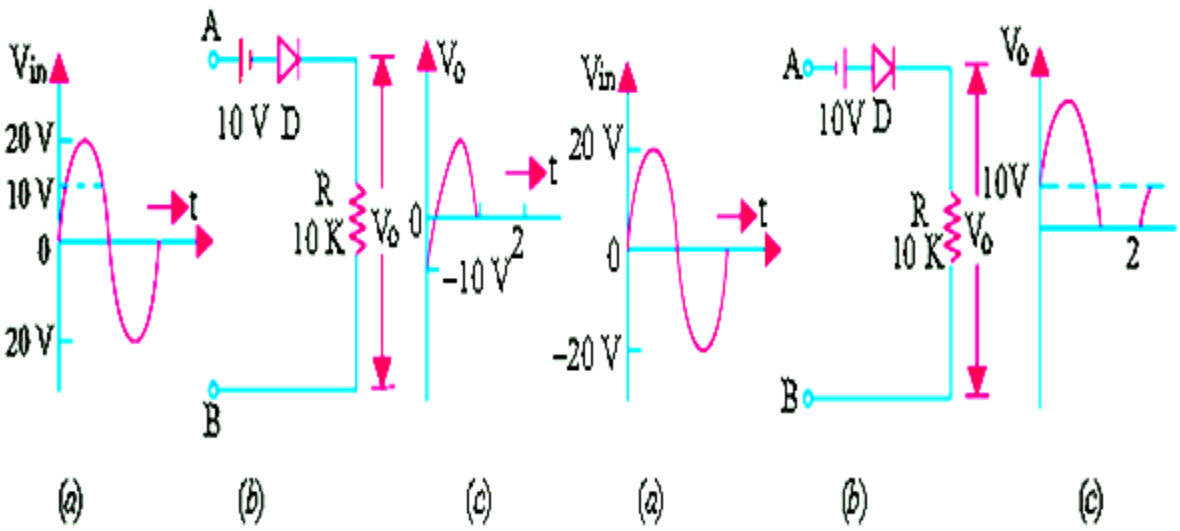
During the positive input half-cycle when point *A* is positive, diode becomes reverse-biased and hence, becomes open-circuited. The applied voltage drops across the resistors *R* and *RL* connected in series. The peak value of the output voltage is

$$V_p = 15 \times \frac{R_L}{R + R_L}$$

$$= 15 \times \frac{1}{1.1} = 13.64\,V.$$

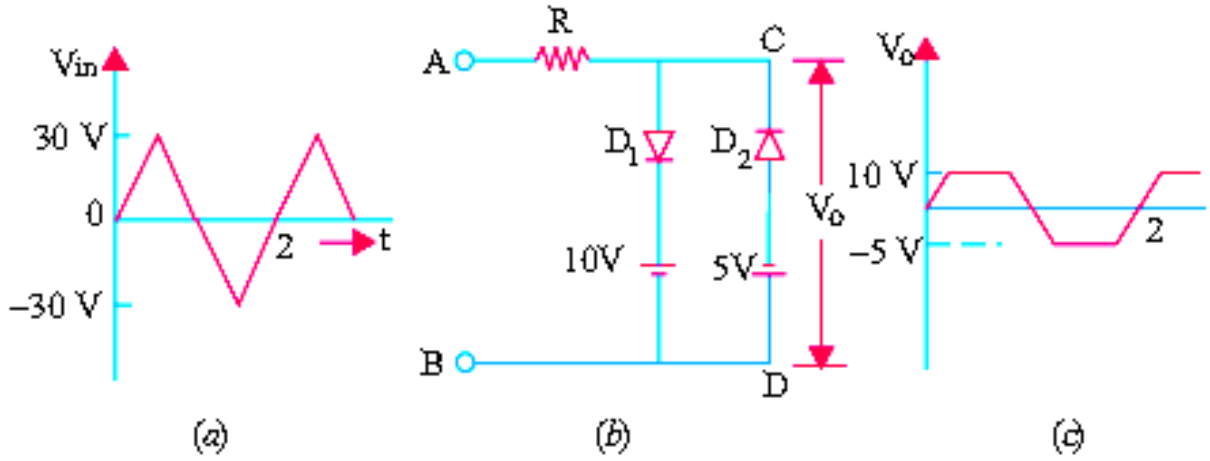
Example:

With the sine wave signal input of Fig. below (a) find the shape of the output signal V_0. (b) Find the shape of the output signal V_0. if battery connections are reversed and peak value of the output voltage.



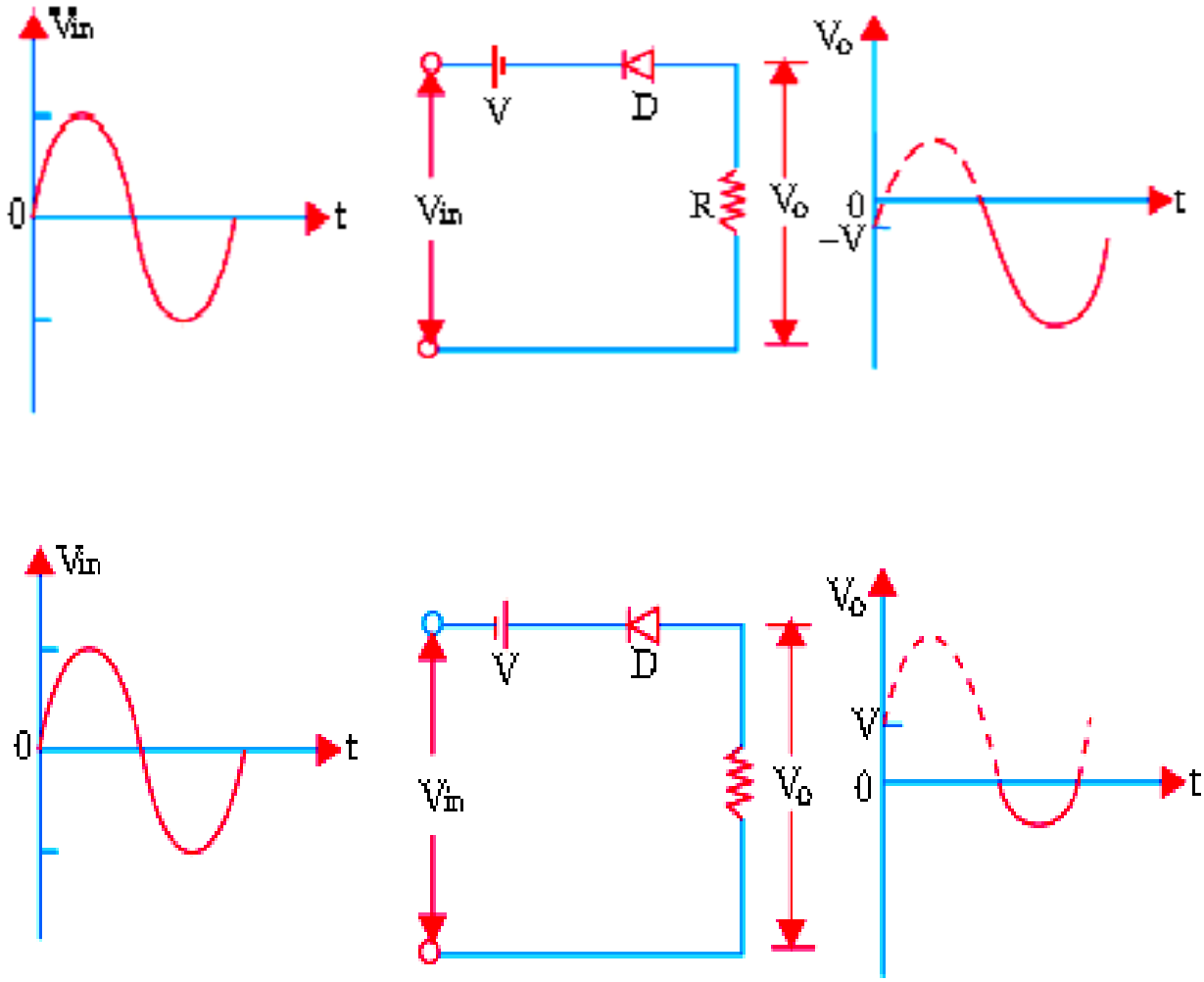
Example:

The triangular voltage of Fig. below (a) is applied to the biased parallel Clipper circuit of Fig. below (b). Find the wave-shape of the output voltage together with the maximum value of the output.



(*a*) Biased Series Clippers

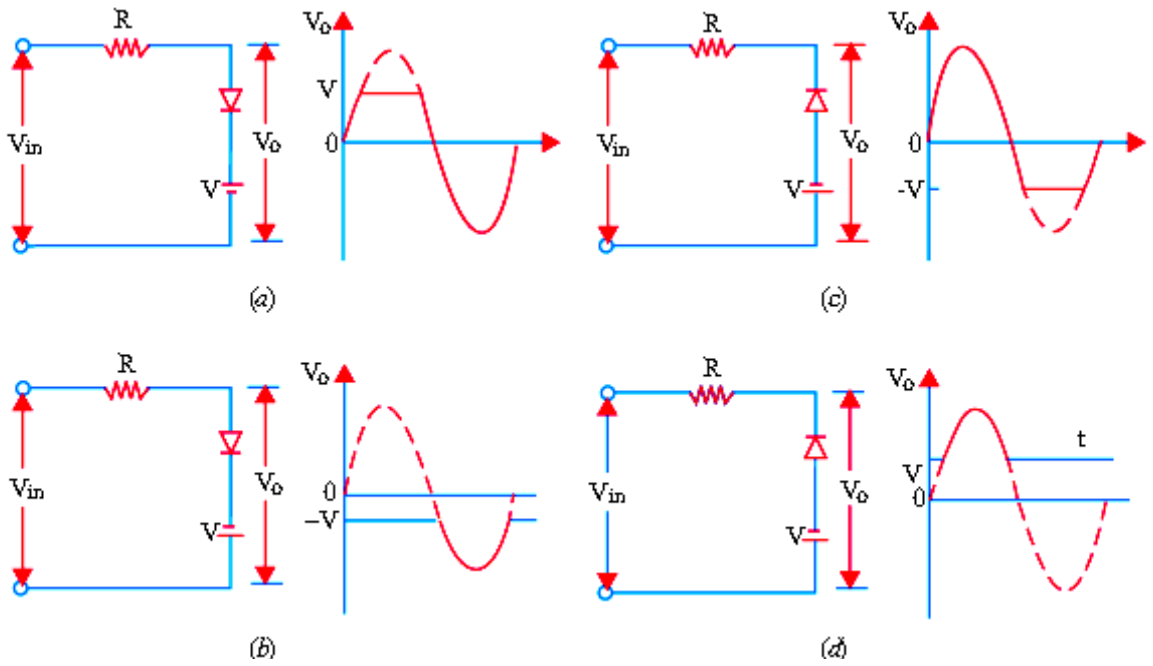
Consider the wave form shown below, and then the output voltage of the biased series circuits will be as shown below:



(b) Biased Parallel Clippers

The waveforms of the output voltage are as shown below:

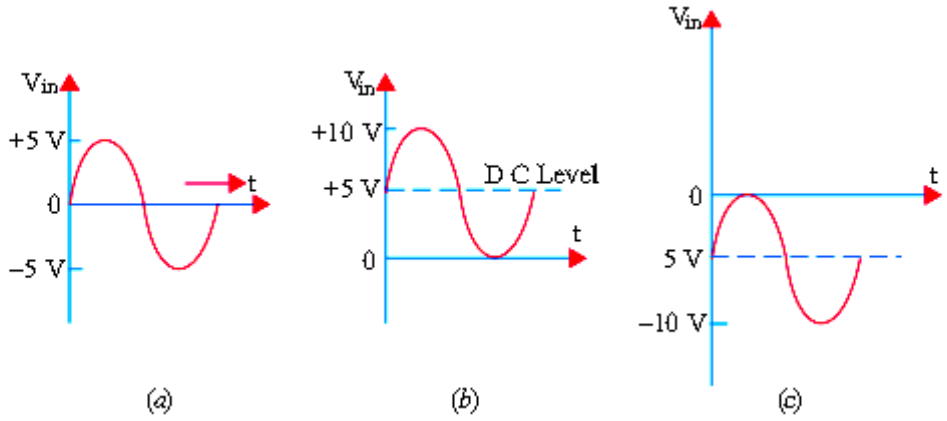
Clipping has been changed by changing the battery and diode connections.



Clampers

To put it simply, clamping is the process of introducing a dc level into an ac signal. Clampers are also sometimes known as dc restorers.

By way of illustration, consider the signal shown in Fig. below (*a*). It is a sine wave with equal of ± 5 V about 0 V.



A clamper circuit has a minimum requirement of three elements, diode**,** capacitor and resistor. Also it needs a dc battery. Following additional points regarding clamper circuits are worth keeping in mind.

1. Both R and C affect the waveform.

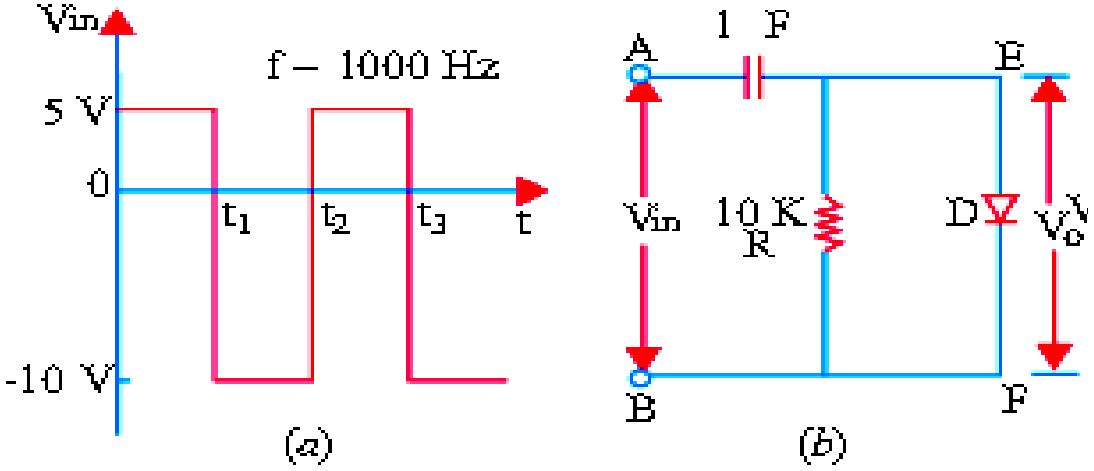
2. Values of R and C should produce a time constant (τ= CR) which is large enough to ensure that capacitor remains almost fully charged during the time-period of the signal. In other words, time constant τ» T/2 where T is the time-period of the input signal. For good clamping action, the RC time constant should be at least ten times the time-period of the input signal voltage.

3. It is advantageous to first consider the condition under which the diode becomes forward biased.

4. For all clamping circuits, voltage swing of the input and output wave forms is the same.

Example:

The input signal of Fig. below (a) is applied to the clamper circuit shown in Fig. below (b). Draw the waveform of the output voltage V_0. How will it change if R is 100 Ω?



Solution:

As seen, time-period of the input signal is T = 1/1000 second = 1 ms

T/2 = 0.5 ms.

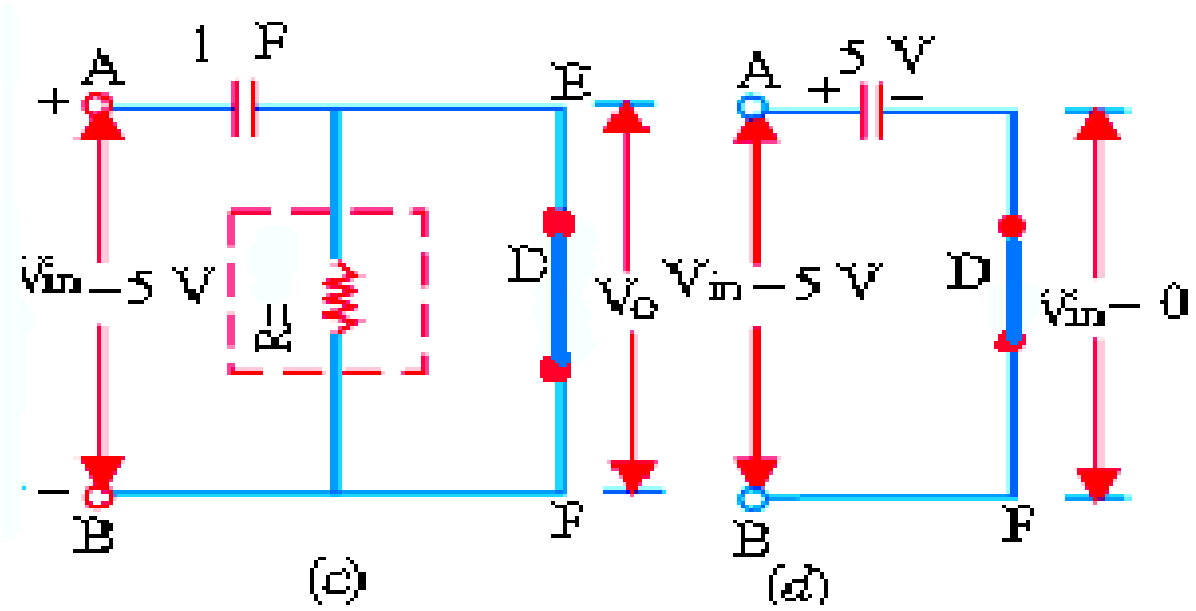
$\tau = 1 \times 10{-}6 \times 10 \times 103 = 10$ ms

τ » T/2. Hence, once charged, the capacitor will have hardly any time to discharge by the time signal polarity reverses.

We consider the two half cycles of the input signal separately:

(*a*) Positive Input Half-cycle

When positive half-cycle of the input signal voltage is applied to the clamper circuit, its terminal *A* becomes positive with respect to terminal *B*. Hence, *D* acts like a short as shown in Fig. below(*c*). A steady positive voltage of 5 V remains applied to *A* for 0.5 ms. at the same time, *R* is also shorted out because it is in parallel with *D*. Hence, C will rapidly charge to 5 V. Being across a short, $V_0 = 0$ during positive half-cycle as shown below.

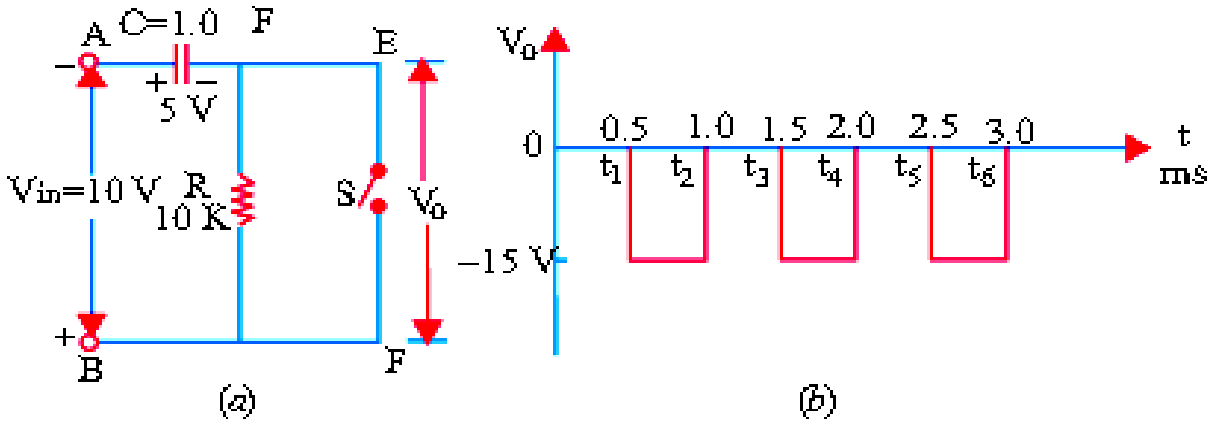


(*b*) Negative Input Half-cycle

In this case, terminal *B* becomes positive and so reverse-biases *D* by 10 V. Hence, *D* acts like an open switch as shown below. Now, *R* and *C* get connected in series

so that their $\tau = RC$ = 10 ms. as stated earlier, capacitor will take a time of 5τ = 50 ms to get fully discharged. But the input signal will allow it just 0.5 ms during which to discharge. Obviously, *C* would hardly get discharged in this extremely short time interval of 0.5 ms. hence, it can be assumed to be still fully charged with the original polarity during this negative half-cycle.

The output voltage V_0 across the 'open' will be = voltage from $E \rightarrow A \rightarrow B \rightarrow F$ – = 5 + 10 = 15 V – with *E* negative the waveform of the output voltage is shown in Fig. below (*b*). It has same frequency as that of the input signal. However, it has been clamped down in the negative region. It is seen that voltage swing of both input and output circuits is the same *i.e.* 15 V.

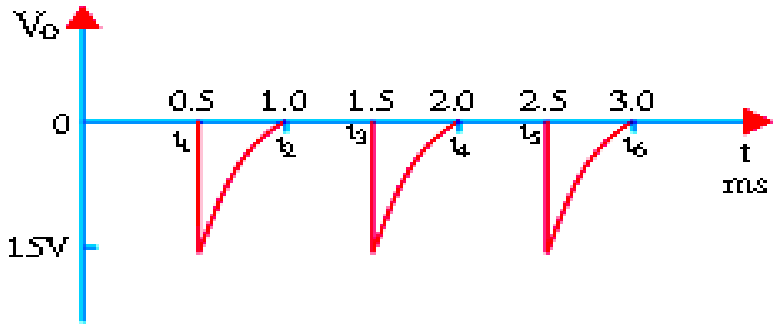


When R = 100Ω

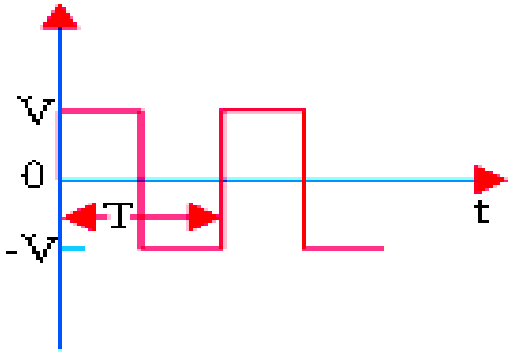
Now, $\tau = 100 \times 1 \times 10^{-6}$ ms = 0.1 ms. hence, the capacitor which is almost instantaneously charged to +5 V during the positive input half-cycle, will be

almost completely discharged during the negative half cycle because, now, 5 τ (full discharge time) equals the half time-period (0.5 ms) of the signal.

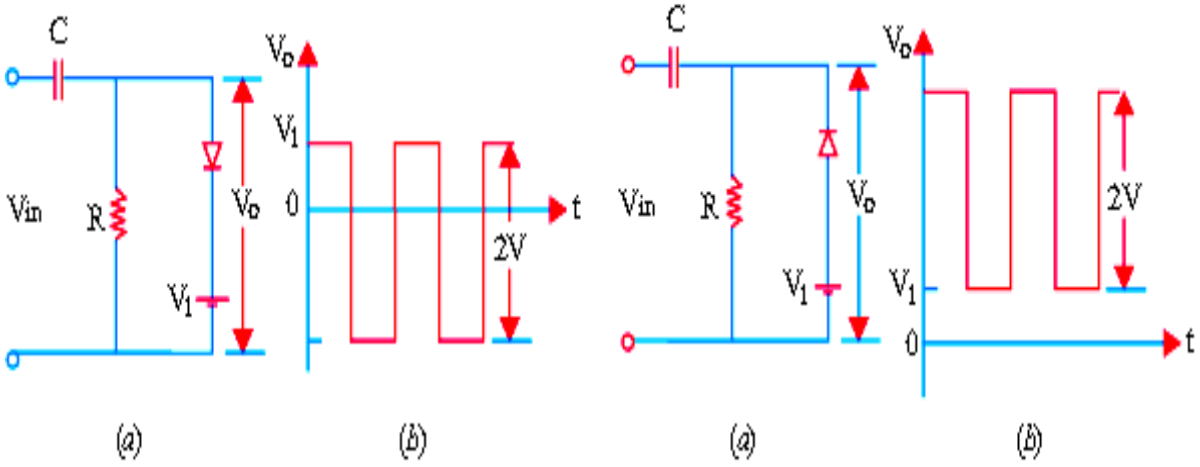
Hence, in this case, V_0 would be momentarily equal to – 15 V at the beginning of the negative half-cycle but will fall off to almost 0 V before the signal reverses its polarity (Fig. below). As seen, υ_0 consists of voltage spikes of amplitude –15 V.

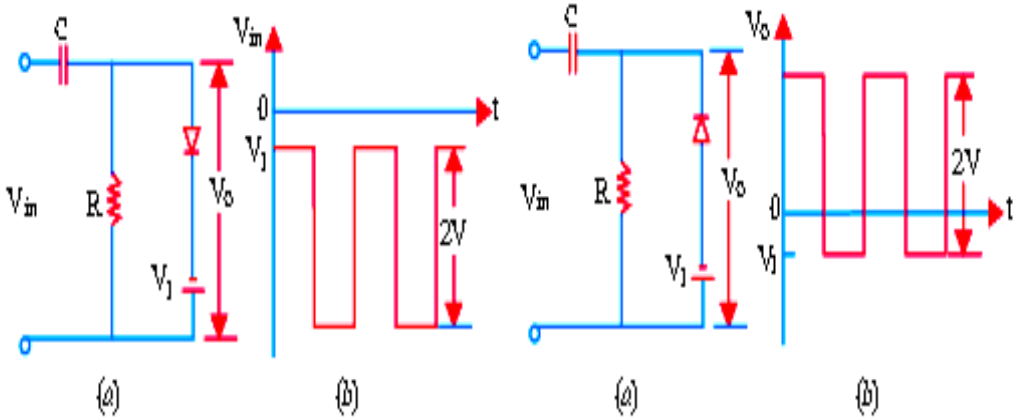


In the following clamping circuits, it would be assumed that the amount of the time $5\tau = 5\ RC \gg T/2$ where T is the time-period of the input signal. For all circuits, we will take the same input signal shown below with a peak value of V. We will also take note of the change in the output waveform when diode connections are reversed.



Input signal


C
Vin
R
Vo
V1
Vo
V1
0
t
2V
(a)
(b)
C
Vo
Vin
R
Vo
V1
V1
2V
0
t
(a)
(b)


C
Vin
R
Vo
V1
Vin
0
t
V1
2V
(a)
(b)
C
Vo
Vin
R
Vo
V1
2V
0
t
V1
(a)
(b)

SPECIAL DIODES

Zener Diode

It is a reverse-biased heavily-doped silicon (or germanium) P-N junction diode which is operated in the breakdown region where current is limited by both external resistance and power dissipation of the diode. Silicon is preferred to Ge because of its higher temperature and current capability.

When a diode breaks down, both Zener and avalanche effects are present although usually one or the other predominates depending on the value of reverse voltage. At reverse voltages less than 6 V, Zener effect predominates whereas above 6 V, avalanche effect is predominant. Strictly speaking, the first one should be called Zener diode and the second one as avalanche diode but the general practice is to call both types as Zener diodes.

Zener breakdown occurs due to breaking of covalent bonds by the strong electric field set up in the depletion region by the reverse voltage. It produces an extremely large number of electrons and holes which constitute the reverse saturation current (now called Zener current, I_z) whose value is limited only by the external resistance in the circuit. It is independent of the applied voltage.

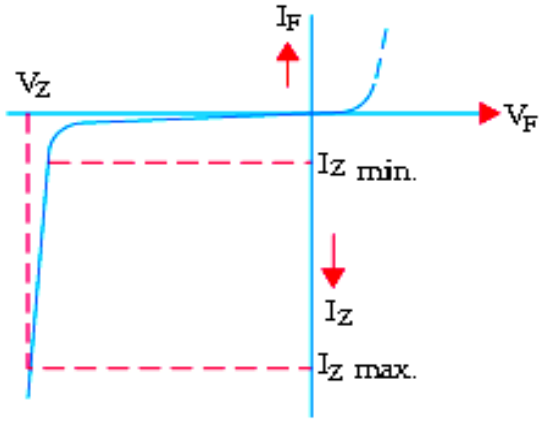
(a) V/I Characteristic

A typical characteristic is shown by Fig. below in the negative quadrant. The forward characteristic is simply that of an ordinary forward-biased junction diode. The important points on the reverse characteristic are:

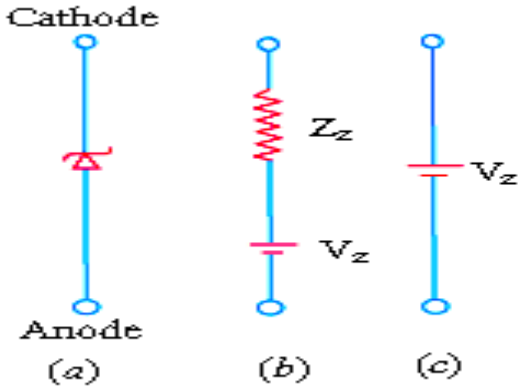
V_z = Zener breakdown voltage

I_z min = minimum current to sustain breakdown

I_z max = maximum Zener current limited by maximum power dissipation.



The schematic symbol of a Zener diode and its equivalent circuit are shown in Fig. below.



(b) Zener Voltages

Zener diodes are available having Zener voltages of 2.4 V to 200 V. Their power dissipation is given by the product V_zI_z. Maximum ratings vary from 150 mW to 50 W.

(c) Zener Biasing

For proper working of a Zener diode in any circuit, it is essential that it must

1. be reverse-biased.
2. Have voltage across it greater than V_z.
3. be in a circuit where current is less than I_z *max.*

(*d*) Uses

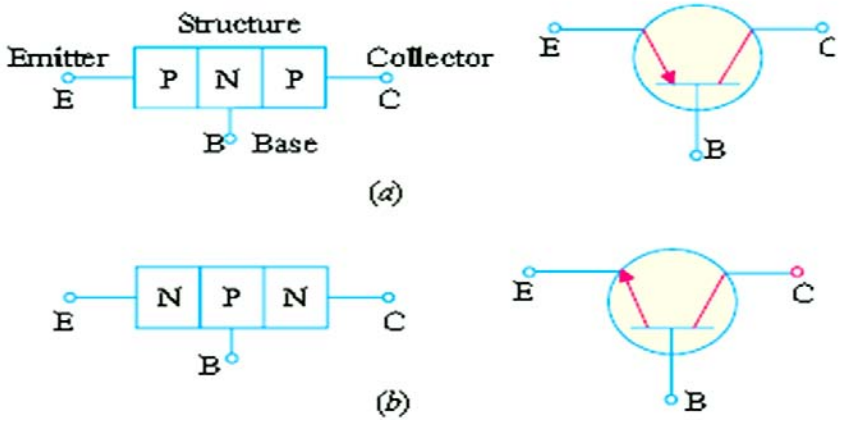
Zener diodes find numerous applications in transistor circuitry. Some of their common uses are:

1. as voltage regulators.
2. as a fixed reference voltage in a network for biasing and comparison purposes and for calibrating voltmeters.
3. as peak clippers or voltage limiters.
4. for meter protection against damage from accidental application of excessive voltage.
5. for reshaping a waveform.

Transistors

1. Introduction to transistor circuit:

Basically, the transistor consists of two back-to back P-N junctions manufactured in a single piece of a semiconductor crystal. These two junctions give rise to three regions called emitter, base and collector. As shown in Fig. 1 (a) junction transistor is simply a sandwich of one type of semiconductor material between two layers of the other type. Fig. 1 (a) shows a layer of N-type material sandwiched between two layers of P-type material. It is described as a PNP transistor. Fig. 1 (b) shown an NPN – transistor consisting of a layer of P-type material sandwiched between two layers of N-type material. The emitter, base and collector are provided with terminals which are labelled as E, B and C. The two junctions are: emitter-base (E/B) junction and collector-base (C/B) junction. The symbols employed for PNP and NPN transistors are also shown in Fig. 1. For a PNP transistor, arrowhead points from emitter to base meaning that emitter is positive with respect to base (and also with respect to collector)* For NPN transistor, it points from base to emitter meaning that base (and collector as well)* is positive with respect to the emitter.



1. Emitter

It is more heavily doped than any of the other regions because its main function is to supply majority charge carries (either electrons or holes) to the base.

2. Base

It forms the middle section of the transistor. It is very thin (10^{-6} m) as compared to either the emitter or collector and is very lightly-doped.

3. Collector

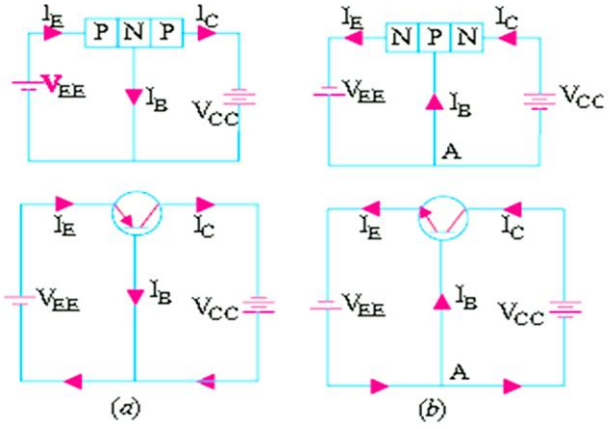
Its main function (as indicated by its name) is to collect majority charge carriers coming from the emitter and passing through the base.

2. Transistor Biasing

For proper working of a transistor, it is essential to apply voltages of correct polarity across its two depletion layers one with each junctions. These layers form a barrier which is need some positional to breaking this potential is 0.7 V. for Si junction and 0.3 V. for Ge junction. For the normal operation of the transistor ,the following should be verified:

1. emitter-base junction is always forward biased and
2. collector-base junction is always reverse- biased.

This type of biasing is known as reverse biasing. As showing in fig. (3-a, b)



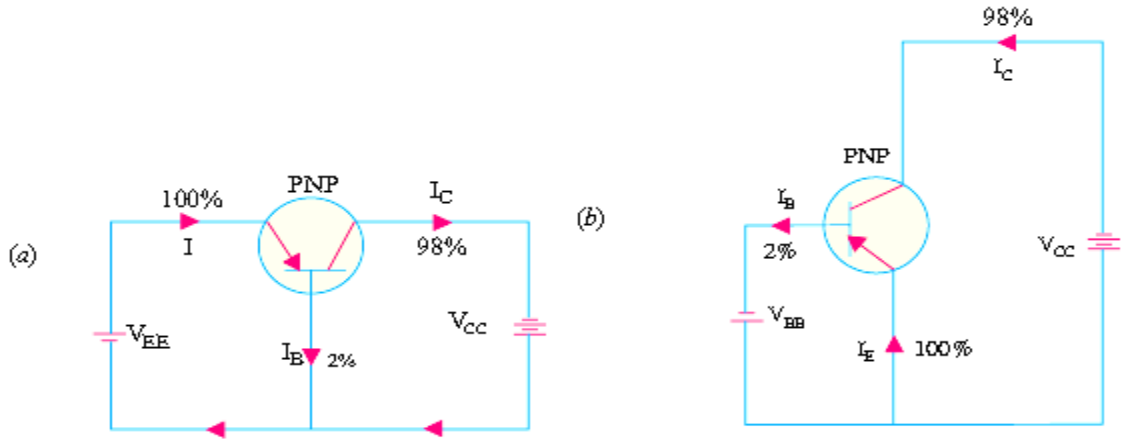
Positive terminal of V_{EE} is connected to P-type emitter in order to repel or Push holes into the base. The negative terminal of V_{CC} is connected to the collector so that it may attract or pull holes through the base. Similar considerations apply to the NPN transistor. It must be remembered that a transistor will never conduct any current if its emitter-base junction is not forward- biased.

4. Transistor Currents:

The three primary currents which flow in a properly-biased transistor are I_E, I_B and I_C. In Fig. 4 (a) are shown the directions of flow as well as relative magnitudes of these currents for a PNP transistor connected in the common-base mode. It is seen that again, $I_E = I_B + I_C$

It means that a small part (about 1—2%) of emitter current goes to supply base current and the remaining major part (98—99%) goes to supply collector current. Moreover, I_E flows into the transistor whereas both I_B and I_C flow out of it.

Fig. 4 (b) shows the flow of currents in the same transistor when connected in the common-emitter mode. It is seen that again, $I_E = I_B + I_C$ this can be proved by taking current flowing in to a transistor are positive. $I_E + (-I_B) + (-I_C) = 0$ or $I_E = I_B + I_C$. This statement is true regardless of transistor type or transistor configuration.



Note.

The four basic guideposts about all transistor circuits are:

1. Conventional current flows along the arrow whereas electrons flow against it;
2. E/B junction is always forward-biased;
3. C/B junction is always reverse-biased;
4. $I_E = I_B + I_C$.

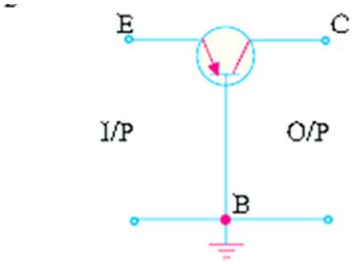
6. Transistor Circuit Configurations

Basically, there are three types of circuit connections (called configurations) for operating a transistor.

1. Common-base (CB),
2. Common-emitter (CE),
3. Common-collector (CC).

-Common-base (CB) Configuration

The input signal is applied between the emitter and base whereas output is taken out from the collector.



The ratio of the collector current to the emitter current is called dc alpha (α_{dc}) of a transistor.

$$\alpha_{dc}^{*} = \frac{-I_C}{I_E}$$

$$I_C = -\alpha_{dc} . I_E$$

It is also called forward current transfer ratio ($-h_{FB}$). If we neglect (-) the $\alpha = I_E / I_C$ .The α of a transistor is a measure of the quality of a transistor; higher the value of α, better the transistor in the sense that collector current more closely equals the emitter current.

$I_C = \alpha I_E$ Now, $I_B = I_E - \alpha I_E = (1 - \alpha) I_E$

There is also an $\alpha_{a.c}$. for a transistor.

$$\alpha_{ac} = \frac{-\Delta I_C}{\Delta I_E}$$

It is also, known as short-circuit gain of a transistor and is written as $-h_{fb}$. For all practical purposes, $\alpha_{dc} = \alpha_{ac} = \alpha$.

Example: in a transistor connected as a CB configuration: $I_E = 2$ mA and $I_B = 20$ μA. Compute the values of α and IC.

Solution: $I_C = I_E - I_B = 2 \times 10^{-3} - 20 \times 10^{-6} = 1.98$ mA

$\alpha = I_C / I_E = 1.98/2 = 0.99$

- **Common-emitter CE Configuration**

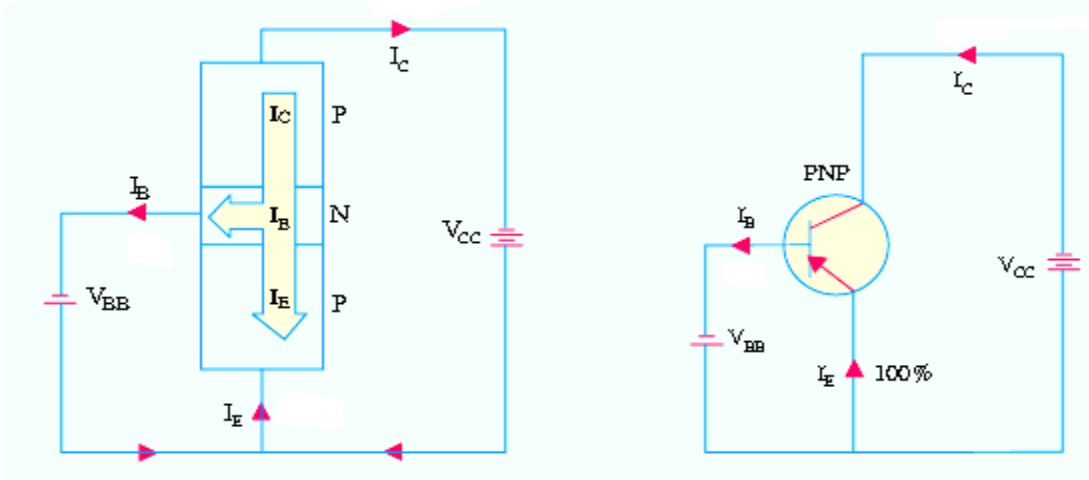
Here, input signal is applied between the base and emitter and output signal is taken out from the collector and emitter circuit. As seen from Fig. below, I_B is the input current and I_C is the output current.

$\beta = -I_C / -I_B = I_C / I_B$ or $I_C = \beta I_B$

It is also called common-emitter d.c. forward transfer ratio and is written as h_{FE}. While analysing ac operation of a transistor, we use ac β which is given by $\beta_{ac} = \Delta I_C / \Delta I_B$. It is also written as h_{fe}.

The flow of various currents in a *CE* configuration both for *PNP* and *NPN* transistor is shown in Fig. below.

$$I_E = I_B + I_C = I_B + \beta I_B = (1 + \beta)\, I_B$$



- **Relation Between α and β**

$$\beta = \frac{I_C}{I_B} \quad \text{and} \quad \alpha = \frac{I_C}{I_E} \quad \therefore \quad \frac{\beta}{\alpha} = \frac{I_E}{I_B}$$

Now, $I_B = I_E - I_C$ $\therefore$ $\beta = \dfrac{I_C}{I_E - I_C} = \dfrac{I_C / I_E}{I_E / I_E - I_C / I_E}$

or $\beta = \dfrac{\alpha}{1 - \alpha}$

$\beta\,(1 - a) = \alpha$ or $\beta = \alpha\,(1 + \beta)$

$\alpha = \beta / (1 + \beta)$

$1 - \alpha = 1/(1 + \beta)$

- **CC Configuration**

In this case, input signal is applied between base and collector and output signal is taken out from emitter-collector circuit I_B is the input current and I_E is the output

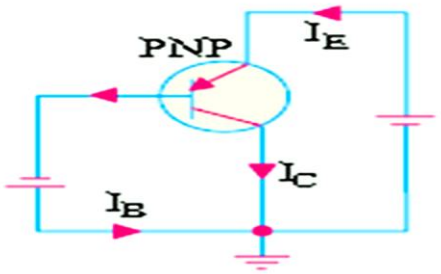
$$\frac{I_E}{I_B} = \frac{I_E}{I_C} \cdot \frac{I_C}{I_B} = \frac{\beta}{\alpha} = \frac{\beta}{\beta/(1+\beta)} = (1+\beta)$$

current The current gain of the circuit is it means that o/p current is (1+β) times the i/p current.

The flow paths of various currents in a CC configuration are

$$I_E = I_B + I_C = I_B + \beta I_B = (1+\beta) I_B$$

$$\therefore \text{ output current} = (1+\beta) \times \text{input current}$$



- **Relations Between Transistor Currents:**

$$\alpha = \frac{I_C}{I_E}, \qquad \beta = \frac{I_C}{I_B}$$

$$\alpha = \frac{\beta}{(1+\beta)} \text{ and } \beta = \frac{\alpha}{(1-\alpha)}$$

(i) $$I_C = \beta I_B = \alpha I_E = \frac{\beta}{1+\beta} I_E$$

(ii) $$I_B = \frac{I_C}{\beta} = \frac{I_E}{1+\beta} = (1-\alpha) I_E$$

(iii) $$I_E = \frac{I_C}{\alpha} = \frac{1+\beta}{\beta} I_C = (1+\beta)\, I_B = \frac{I_B}{(1-\alpha)}$$

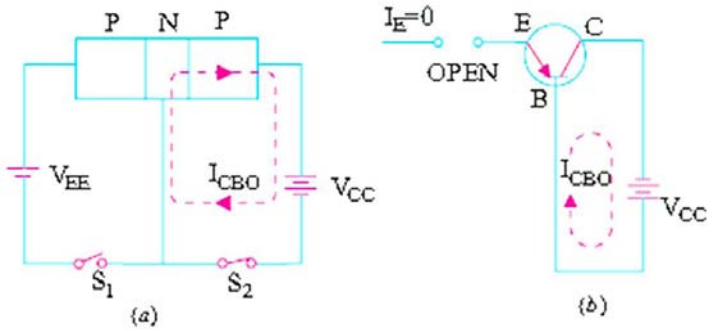
Leakage Currents in a Transistor

(a) CB Circuit

Consider the CB transistor circuit shown in Fig. below. The emitter current (due to majority carriers) initiated by the forward-biased emitter base junction is split into two parts :

(i) $(1 - \alpha)\, I_E$ which becomes base current I_B in the external circuit and

(ii) $\alpha\, I_E$ which becomes collector current I_C in the external circuit.



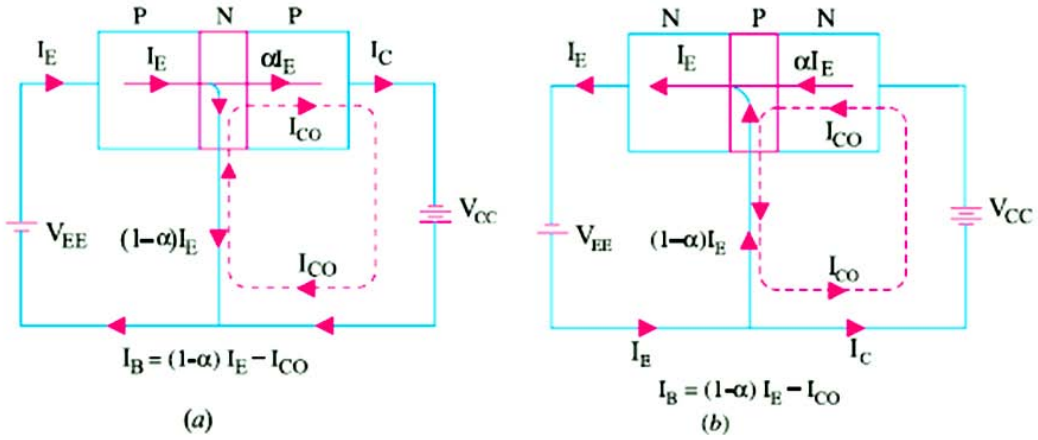
As mentioned earlier, though C/B junction is reverse-biased for majority charge carriers(i.e. holes in this case), it is forward-biased so far as thermally-generated minority charge carriers (i.e. electrons in this case) are concerned. These current flows even when emitter is disconnected from its dc supply as shown in Fig. below (a) where switch, S_1 is open. It flows in the same direction* as the collector current of majority carriers. It is called leakage current I_{CBO}. The subscripts CBO stand for 'Collector to Base with emitter Open.' Very often, it is simply written as I_{CO}.

It should be noted that

(i) I_{CBO} is exactly like the reverse saturation current I_S or I_0 of a reverse-biased diode discussed

(ii) I_{CBO} is extremely temperature-dependent because it is made up of thermally-generated minority carriers. As mentioned earlier, I_{CBO} doubles for every 10°C rise in temperature for Ge and 6°C for Si.

If we take into account the leakage current, the current distribution in a CB transistor circuit becomes as shown in Fig. below both for PNP and NPN type transistors.



It is seen that total collector current is actually the sum of two components:

(i) Current produced by normal transistor action i.e. component controlled by emitter current. Its value is a I_E and is due to majority carriers.

(ii) temperature-dependent leakage current I_{CO} due to minority carriers.

$$\therefore \quad I_C = \alpha I_E + I_{CO} \qquad \ldots(i) \qquad \therefore \quad \alpha = \frac{I_C - I_{CO}}{I_E}$$

Since $I_{CO} \ll I_C$, hence $\alpha \cong I_C / I_E$

(iii) Substituting the value of $I_E = (I_C + I_B)$ in Eq. (i) above, we get

$$I_C = (I_C + I_B) + I_{CO} \qquad \text{or} \qquad I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$\therefore \quad I_C = \frac{\alpha I_B}{1-\alpha} + \frac{I_{CO}}{1-\alpha}$$

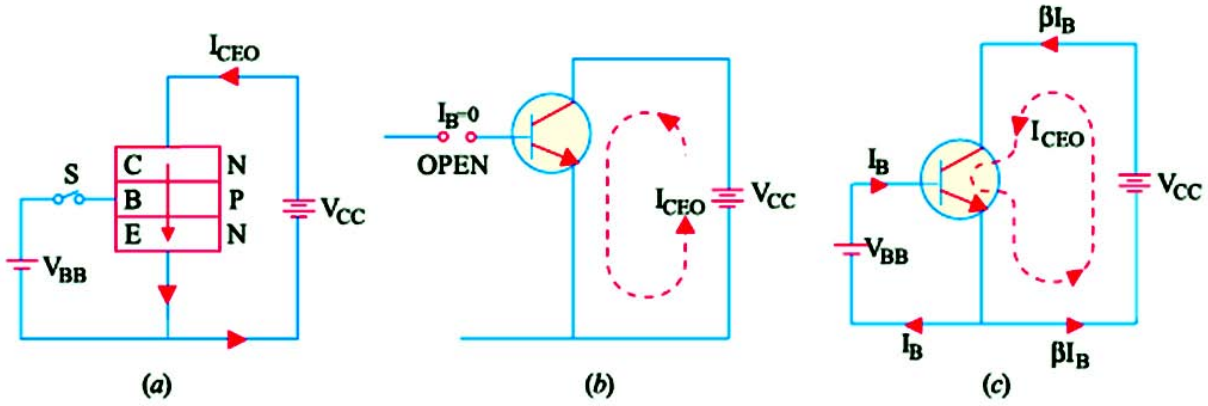
(iv) Eliminating I_C from Eq. (i) above, we get

$$(I_E - I_B) = \alpha I_E + I_{CO} \qquad \text{or} \qquad I_B = (1 - \alpha) I_E - I_{CO}$$

(b) CE Circuit

In Fig. below (a) is shown a common-emitter circuit of an NPN transistor whose base lead is open. It is found that despite $I_B = 0$, there is a leakage current from collector to emitter. It is called I_{CEO}, the subscripts CEO standing for 'Collector to Emitter with base Open'.

Taking this leakage current into account, the current distribution through a CE circuit becomes as shown in Fig. below (c).



$$I_C = \beta I_B + I_{CEO} = \beta I_B + (1 + \beta) I_{CO} = \beta I_B + I_{CO}/(1 - \alpha)$$

(i) $$\therefore \quad I_C = \frac{\alpha I_B}{1 - \alpha} + \frac{I_{CO}}{1 - \alpha}$$

Now, $\beta I_B = \alpha I_E$. Substituting this value above, we get,

$I_C = \alpha I_E + I_{CEO}$ Also, $I_B = I_E - I_C$

Substituting the value of I_C from above, we have

(ii) $I_B = I_E - \alpha I_E - I_{CEO} = (1 - \alpha) I_E - I_{CEO}$

Transistor characteristics and approximation

Transistor Static Characteristics:

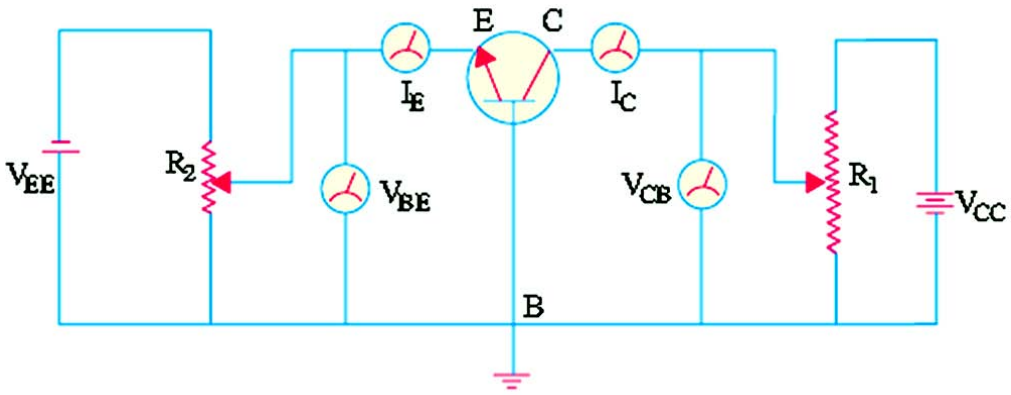
There are the curves which represents relationship between different d.c. currents and voltages of a transistor. The three important characteristics of a transistor are:

1. Input characteristic,

2. Output characteristic,

3. Constant-current transfer characteristic.

Common Base Test Circuit:



Common Base Static Characteristics

(a) Input Characteristic

It shows how I_E varies with V_{BE} when voltage V_{CB} is held constant.

First, voltage V_{CB} is adjusted to a suitable value with the help of R_1 .

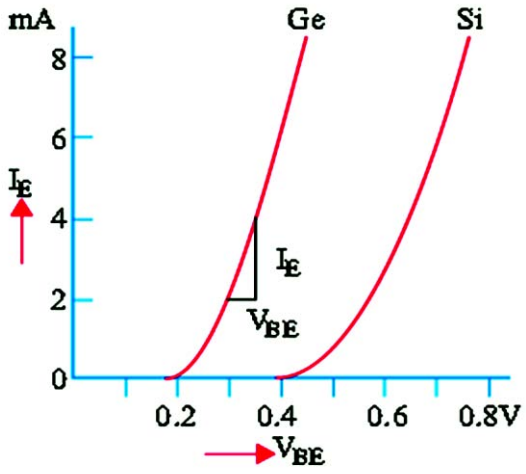
Next, voltage V_{BE} is increased in a number of discrete steps and corresponding values of I_E are noted from the milliammeter.

When plotted, we get the input characteristic shown in Fig. below, one for Ge and the other for Si. Both curves are exactly similar to the forward characteristic of a P-N diode.

This characteristic may be used to find the input resistance of the transistor.

$$R_{in} = \Delta V_{BE} / \Delta I_E \qquad \text{— } V_{CB} \text{ constant.}$$

This characteristic is hardly affected by changes either in V_{CB} or temperature.



(b) Output Characteristic

It shows the way I_C varies with V_{CB} when I_E is held constant.

First, movable contact, on R_2 is changed to get a suitable value of V_{BE} and hence that of I_E. While keeping I_E constant at this value, V_{CB} is increased from zero in a number of steps and the corresponding collector current I_C that flows is noted.

Next, V_{CB} is reduced back to zero, I_E is increased to a value a little higher than before and the whole procedure is repeated. In this way, whole family of curves is obtained.

1. The reciprocal of the near horizontal part of the characteristic gives the output resistance R_{out} of the transistor. R_{out} is very high, a typical value being 500 kΩ.

$$R_{out} = \frac{1}{\Delta I_C / \Delta V_{CB}} = \frac{\Delta V_{CB}}{\Delta I_C}$$

2. It is seen that I_C flows even when $V_{CB} = 0$. For example, it has a value = 1.8 mA corresponding to $V_{CB} = 0$ for $I_E = 2$ mA. It is due to the fact that electrons are being injected into the base under the action of forward-biased E/B junction and are being collected by the collector due to the action of the internal junction voltage at the C/B junction. For reducing I_C to zero, it is essential to neutralize this potential barrier by applying a small forward bias across C/B junction.
3. Another important feature of the characteristic is that a small amount of collector current flows even when emitter current $I_E = 0$. it is collector leakage current I_{CBO}.
4. This characteristic may be used to find α_{ac} of the transistor.

$$\alpha_{ac} = \frac{\Delta I_C}{\Delta I_E} = \frac{DE}{BC}$$

$$= \frac{6.2 - 4.3}{2} = 0.95$$

5. Another point worth noting is that although I_C is practically independent of V_{CB} over the working range of the transistor, yet if V_{CB} is permitted to increase beyond a certain value, I_C eventually increases rapidly due to avalanche breakdown.

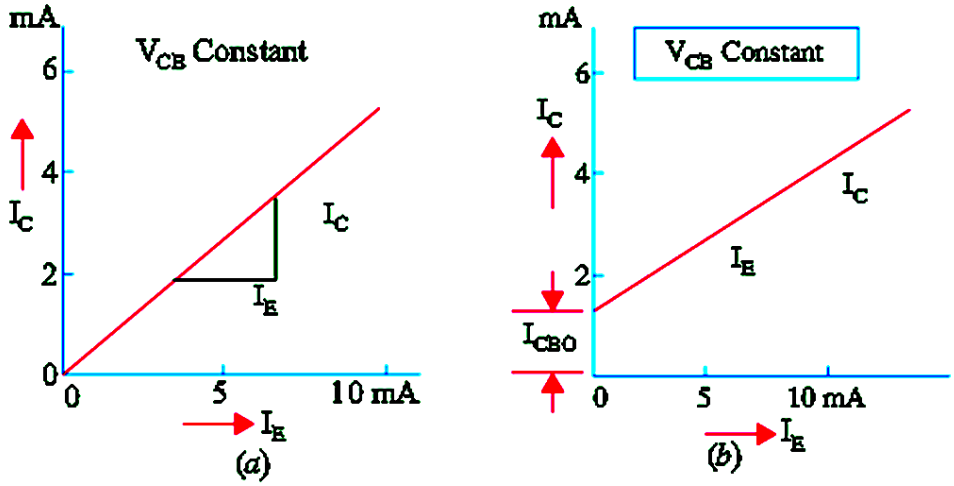
Current Transfer Characteristic

It shows how I_C varies with changes in I_E when V_{CB} is held constant. For drawing this characteristic, first V_{CB} is set to a convenient value and then I_E is increased in steps and corresponding values of I_C noted.

$$\alpha_{ac} = \Delta I_C / \Delta I_E$$

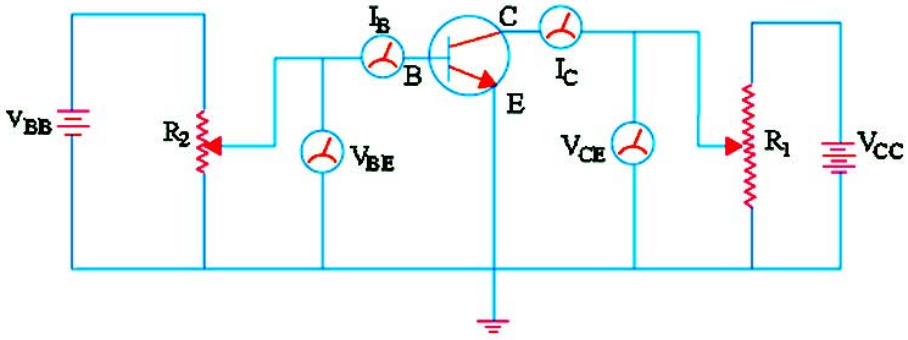
(i) Its current gain is less than unity.

(ii) Its input and output resistances are so different.



Common Emitter Test Circuit

The static characteristics of an NPN transistor connected in CE configuration may be determined by the use of circuit diagram shown in Fig. below.

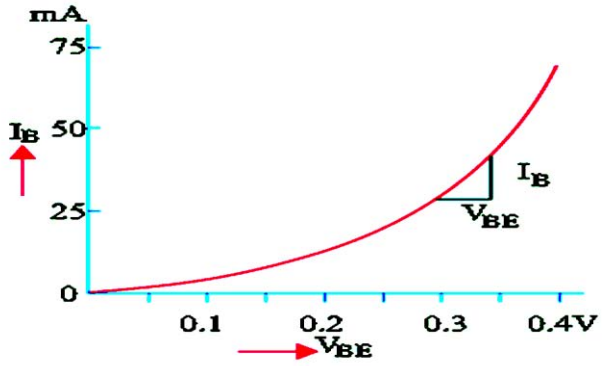


Common Emitter Static Characteristics

(a) Input Characteristic

It shows how I_B varies with changes in V_{BE} when V_{CE} is held constant at a particular value.

$$R_{in} = \frac{\Delta V_{BE}}{\Delta I_B}$$



(b) Output or Collector Characteristic

It indicates the way in which I_C varies with changes in V_{CE} when I_B is held constant.

It is seen that as V_{CE} increases from zero, I_C rapidly increases to a near saturation level for a fixed value of I_B. a small amount of collector current flows even when $I_B = 0$. It is called I_{CEO}. Since main collector current is zero, the transistor is said to be cut-off. If V_{CE} is allowed to increase too far, C/B junction completely breaks down and due to this avalanche breakdown, I_C increases rapidly and may cause damage to the transistor.

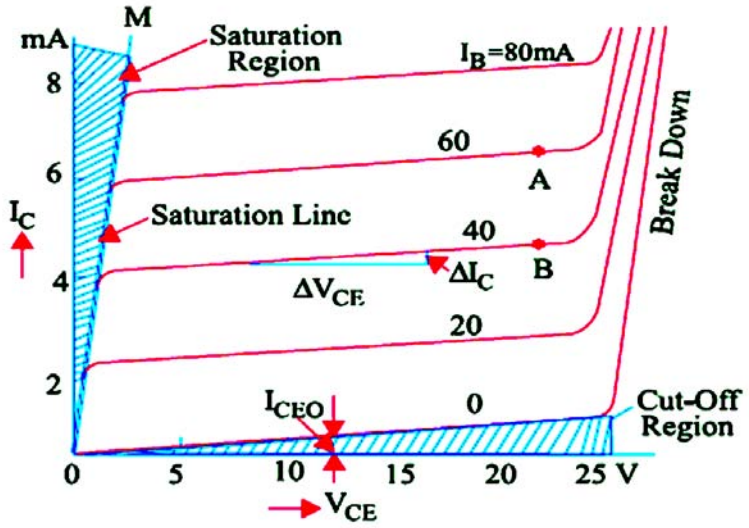
When V_{CE} has very low value (ideally zero), the transistor is said to be saturated and it operates in the saturation region of the characteristic. Here, change in I_B does not produce a corresponding change in I_C.

We can find β_{ac} at a specific value of I_B and V_{CE}.

$$\beta_{ac} = \Delta I_C / \Delta I_B$$

from two points A and B in the fig. below. $\Delta I_B = (60 - 40) = 20\ \mu A$, and we can finding ΔI_C.

R_{out} (= $\Delta V_{CE} / \Delta I_C$) varies from 10 kΩ to 50 kΩ.

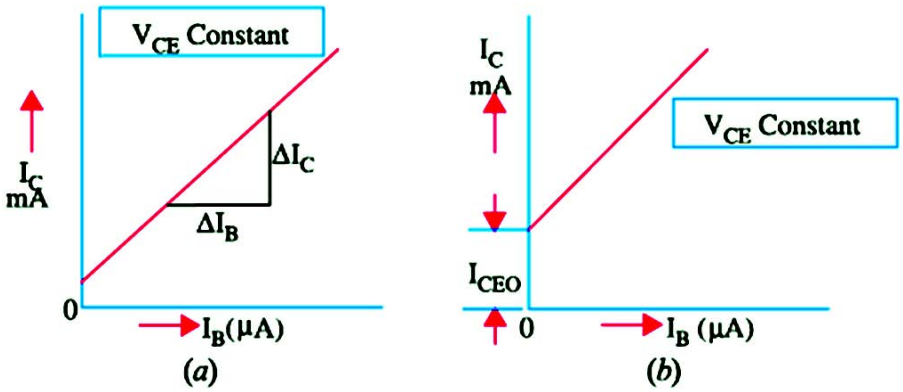


(c) Current Transfer Characteristic

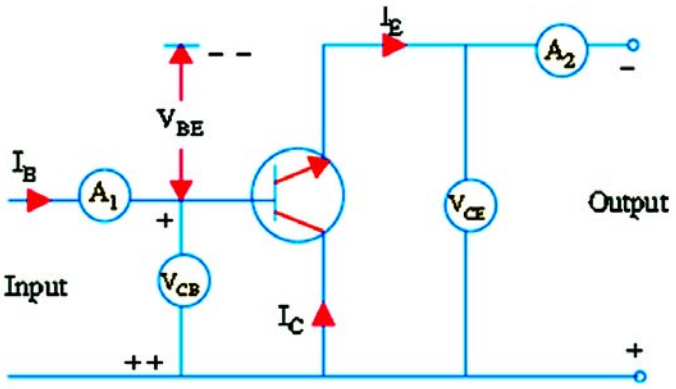
It indicates how I_C varies with changes in I_B when V_{CE} is held constant at a given value. In fig. below (a). The slope gives

$$\beta_{ac} = \Delta I_C / \Delta I_B$$

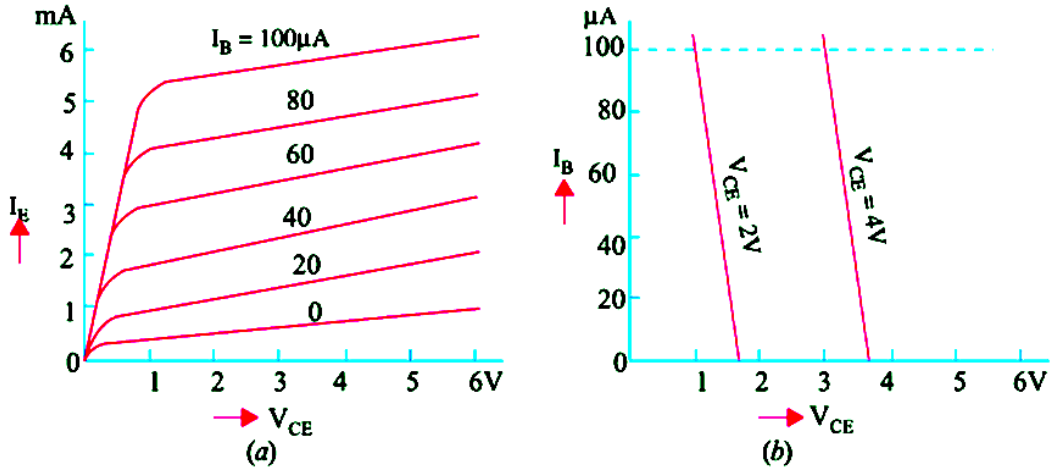
A small collector current flows even when $I_B = 0$. It is the common-emitter leakage current $I_{CEO} = (1 + \beta) I_{CO}$. I_{CO} it is also due to the flow of minority carriers across the reverse-biased C/B junction.



Common Collector Static Characteristics



In this case, collector terminal is common carrier to both the input (CB) and output (CE) carrier's circuits. The output characteristic is I_E versus V_{CE} for several fixed values of I_B. Since $I_C \approx I_E$, as shown in Fig. below (a). The CC input characteristic is a plot of V_{CB} versus I_B for different values of V_{CE} and is shown in fig. below (b).



For I_B = 100 μA and V_{CE} = 2 V.

$V_{CB} = V_{CE} - V_{BE} = 2 - 0.7 = 1.3$ V — for Si material

Moreover, as V_{CB} is increased, V_{BE} is reduced there by reducing I_B. Now, consider the values V_{CE} = 4 V and I_B = 100 μA

$V_{CB} = 4 - 0.7 = 3.3$ V

Again, as V_{CB} increases, I_B is decreased.

Common Base Formulas:

Consider the circuit MEBM. In fig. below, Applying Kirchhoff's voltage law and starting from point B (or ground) upwards, we get

$$(a) \qquad -V_{BE} - I_E R_E + V_{EE} = 0 \qquad \text{or} \qquad I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

where $V_{BE} = 0.3$ V (for *Ge*) and 0.7 V (for *Si*)

Since, generally, $V_{EE} \gg V_{BE}$, we can simplify the above to $I_E \cong V_{EE} / R_E = 10V/20$ K = 0.5 mA

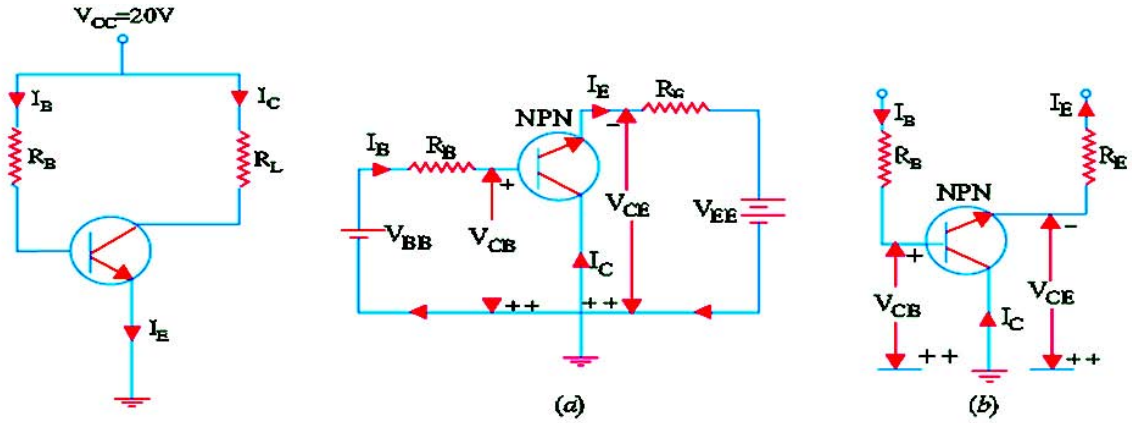
Taking V_{BE} into account and assuming silicon transistor

$$I_E = (10 - 0.7)\ \text{V}/20\ \text{K} = 0.465\ \text{mA}$$

(*b*) $I_C = \alpha I_E \cong I_E = 0.5$ mA neglecting leakage current.

(*c*) From circuit *NCBN*, we get

$$V_{CB} = V_{CC} - I_C \cong V_{CC} - I_E R_L = 25 - 0.5 \times 10 = 20\ \text{V} \qquad (\because I_C \cong I_E)$$



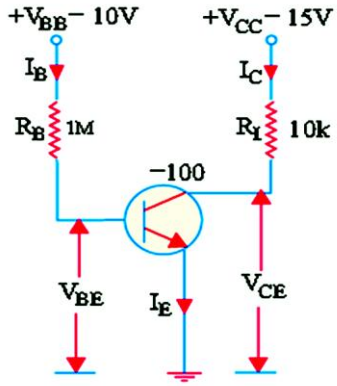
Common Emitter Formulas

Consider the CE circuit of Fig. below. Taking the emitter-base circuit, we have

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} \cong \frac{V_{BB}}{R_B}$$

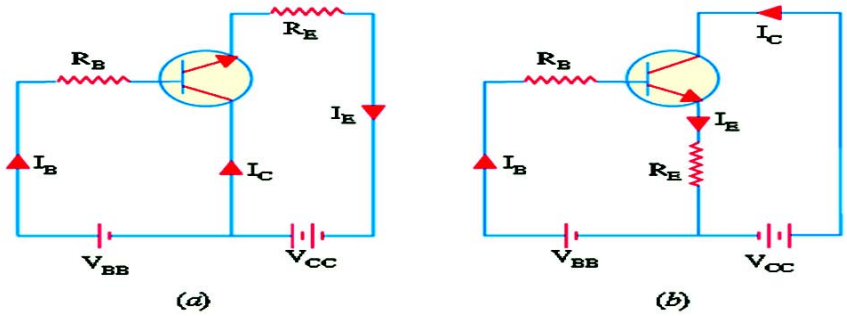
$$I_C = \beta I_B \qquad \text{— neglecting leakage current } I_{CEO}$$

$$V_{CE} = V_{CC} - I_C R_L$$



Common Collector Formulas

The CC circuit with its proper d.c. biasing voltage sources is shown in Fig. below (a). The two circuits given represent the same thing.

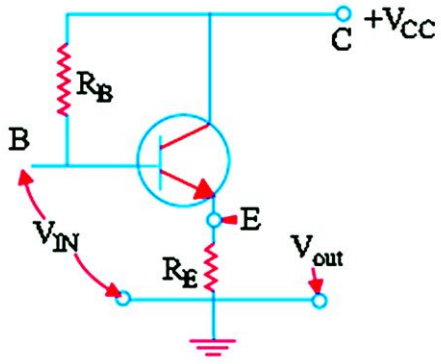


Another way of drawing the same circuit is shown in Fig. below (a) where only one battery has been used. It should be noted that load resistor is not in the collector lead but in the emitter lead as shown.

The fig. below makes the circuit connection quite clear. Input is between base and collector terminals where as output is between emitter and collector terminals.

It is seen that

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + R_B / \beta};$$



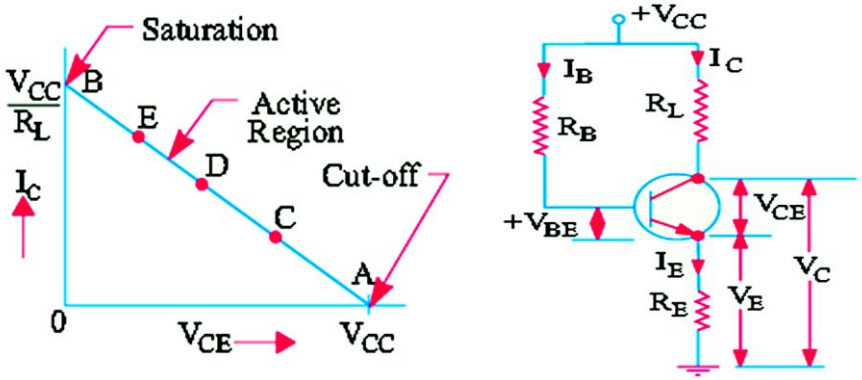
$$V_{CC} = V_{CE} + I_E R_E;$$

$$I_E = \frac{V_{CC} - V_{BE}}{R_E + \beta R_E}; \quad I_C = \beta I_B$$

LOAD LINES AND DC BIAS CIRCUITS

D.C. Load Line

For drawing the dc load line of a transistor, one needs to know only its cut-off and saturation points. It is a straight line jointing these two points. For the CE circuit of Fig. 1, the load line is drawn in Fig. 2.



A is the cut-off point and B is the saturation point. The voltage equation of the collector-emitter is

$$V_{CC} = I_C R_L + V_{CE} \quad \therefore \quad I_C = \frac{V_{CC}}{R_L} - \frac{V_{CE}}{R_L}$$

Consider the following two particular cases :

(*i*) when $I_C = 0$, $V_{CE} = V_{CC}$

— cut-off point A

(*ii*) when $V_{CE} = 0$, $I_C = V_{CC}/R_L$

— saturation point *B*

Load line can be drawn if only V_{CC} and R_L are known.

Active Region

All operating points (like C, D, E etc. in Fig. above) lying between cut-off and saturation points from the active region of the transistor. In this region, E/B junction is forward-biased and C/B junction is reverse-biased.

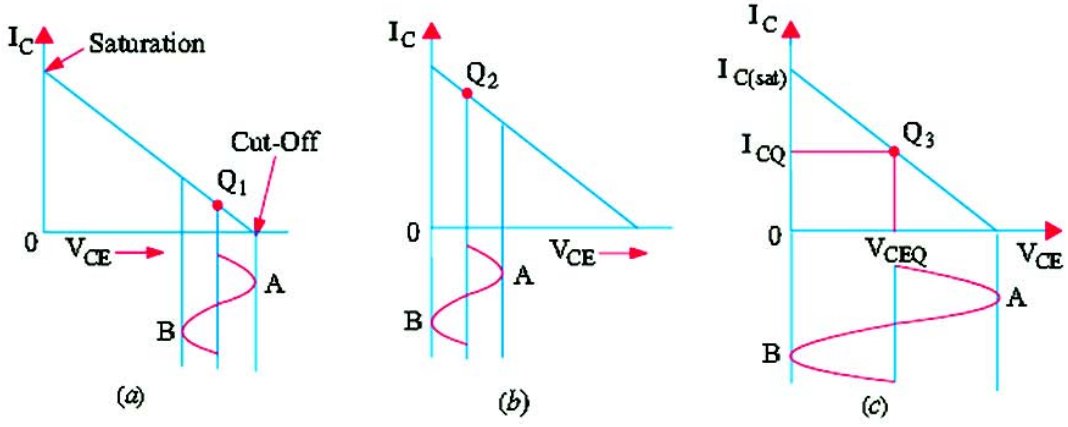
Quiescent Point

It is a point on the dc load line, which represents the values of I_C and V_{CE} that exist in a transistor circuit when no input signal is applied.

It is also known as the dc operating point or working point. The best position for this point is midway between cut-off and saturation points where V_{CE}= ½ V_{CC} (like point D in Fig. above).

Q-Point and Maximum Undistorted Output

Position of the Q-point on the dc load line determines the maximum signal that we can get from the circuit before clipping occurs. Consider the cases shown in Fig. below.

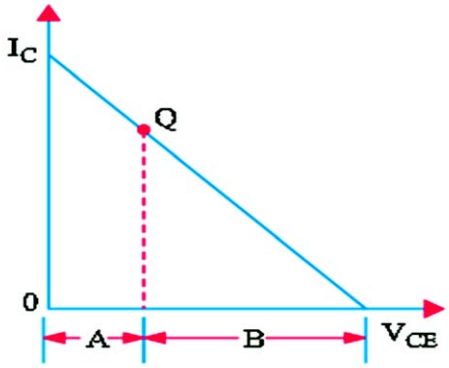


(a) Q_1 is located near cut-off point, signal first starts to clip at A. It is called cut-off clipping because the positive swing of the signal drives the transistor to cut-off. Maximum positive swing is = $I_{CQ}\,R_{ac}$.

(b) Q_2 is located near saturation point, then clipping first starts at point B . It is caused by saturation. The maximum negative swing = V_{CEQ}.

(c) Q_3 is located at the centre of the load line. In this condition, we get the maximum possible output signal. The point Q_3 gives the optimum Q-point. The maximum undistorted signal = $2V_{CEQ}$.

In general, consider the case shown in Fig. 2. Since $A < B$, maximum possible peak-to-peak output signal = 2 A. If the operating point were so located that $A > B$, then maximum possible peak-to-peak output signal = $2B$. When operating point is located at the centre of the load line, then maximum undistorted peak-to-peak signal is = $2A$



$= 2B$

$= V_{CC}$

$= 2 V_{CEQ}$.

Under optimum working conditions corresponding to Fig. 1 (*c*), I_{CQ} is half the saturation value given by V_{CC}/R_L

$$\therefore \quad I_{CQ} = \frac{1}{2} \cdot \frac{V_{CC}}{R_L} = \frac{V_{CC}}{2R}$$

Need For Biasing a Transistor

For normal operation of a transistor amplifier circuit, it is essential that there should be a

(a) Forward bias on the emitter-base junction and

(b) Reverse bias on the collector-base junction.

In addition, amount of bias required is important for establishing the Q-point which is dictated by the mode of operation desired. If the transistor is not biased correctly, it would

1. Work inefficiently and
2. Produce distortion in the output signal.

Factors Affecting Bias Variations

In practice, it is found that even after careful selection, Q-point tends to shift its position. This bias instability is the direct result of thermal instability which itself is produced by cumulative increase in I_C that may, if unchecked, lead to thermal runaway. The collector current for CE circuit is given by

$$I_C = \beta I_B + I_{CEO}$$

$$= \beta I_B + (1 + \beta) I_{CO}$$

This equation has three variables: β, I_B and I_{CO} all of which are found to increase with temperature. In particular, increase in I_{CO} produces significant increase in collector current I_C. This leads to increased power dissipation with further increase in temperature and hence I_C. Being a cumulative process, it can lead to thermal runaway which will destroy the transistor itself.

However, if by some circuit modification, I_C is made to decrease with temperature automatically, then decrease in the term βI_B can be made to neutralize the increase in the term $(1 + \beta) I_{CO}$, thereby keeping I_C constant. This will achieve thermal stability resulting in bias stability.

Stability Factor

The degree of success achieved in stabilizing I_C in the face of variations in I_{CO} is expressed in terms of current stability factor S. It is defined as the rate of change of I_C with respect to I_{CO} when both β and I_B (V_{BE}) are held constant.

$$\therefore \qquad S = \frac{dI_C}{dI_{CO}} \qquad \text{— } \beta \text{ and } I_B \text{ constant}$$

Larger the value of S, greater the thermal instability and vice versa. The stability factor may be alternatively expressed by using the well-known equation

$$I_C = I\,\beta + (I + \beta)\, I_{CO}$$

Which, on differentiation with respect to I_C, yields.

$$I = \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{dI_{CO}}{dI_C}$$

$$= \beta \frac{dI_B}{dI_C} + (1 + \beta) \frac{1}{S}$$

$$\therefore \qquad S = \frac{(1 + \beta)}{1 - \beta (dI_B / dI_C)}$$

Beta Sensitivity

Variations in β-value are caused by variations in the circuit operating conditions or by the substitution of one transistor with another. Beta sensitivity K_β is given by

$$\frac{dI_C}{I_C} = K_\beta \frac{dI_B}{\beta} \qquad \therefore \qquad K_\beta = \frac{\beta}{I_C} \cdot \frac{dI_C}{dI_B}$$

K_β is dimensionless ratio and can have values ranging from zero to unity.

Stability Factor for CB and CE Circuits

(*i*) CB Circuit

Here, collector current is given by

$$I_C = \alpha I_E + I_{CO} \qquad \therefore \qquad \frac{dI_C}{dI_{CO}} = 0 + 1 \qquad \text{or} \qquad S = 1$$

(*ii*) CE Circuit

$$I_C = \beta I_B + (1 + \beta)\, I_{CO} \qquad \therefore \quad \frac{dI_C}{dI_{CO}} = (1+\beta) \qquad \text{—treating } I_B \text{ as a constant}$$

$$\therefore \qquad S = (1 + \beta).$$

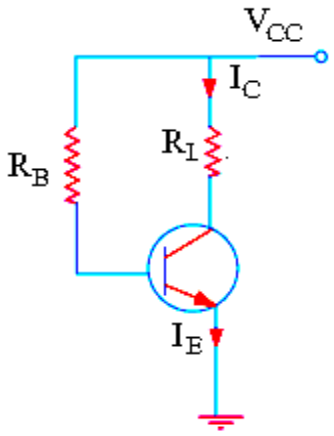
If β = 100, then S = 101 which means that I_C changes 101 times as much as I_{CO}.

Different Methods for Transistor Biasing

Some of the methods used for providing bias for a transistor are:

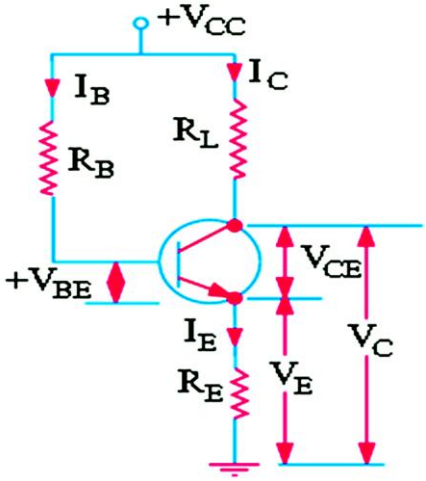
1. Base bias or fixed current bias.

It is not a very satisfactory method because bias voltages and currents do not remain constant during transistor operation.



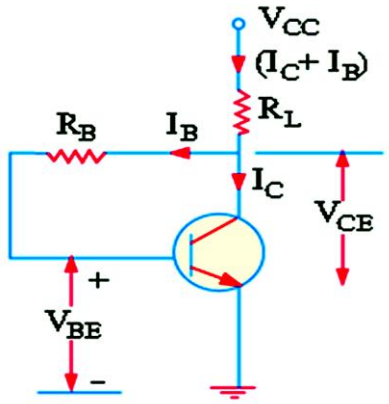
2. Base bias with emitter feedback.

This circuit achieves good stability of dc operating point against changes in β with the help of emitter resistor which causes degeneration to take place.



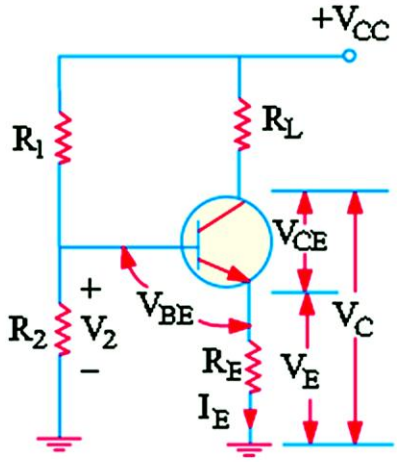
3. Base bias with collector feedback.

It is also known as collector-to-base bias or collector feedback bias. It provides better bias stability.



4. Voltage divider bias.

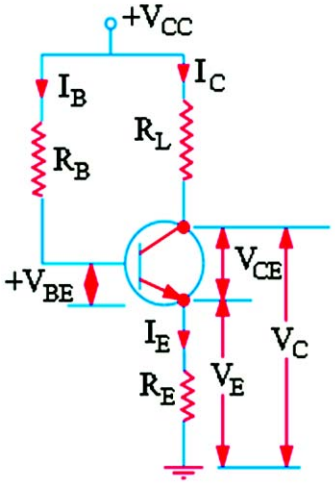
It is most widely used in linear discrete circuits because it provides good bias stability. It is also called universal bias circuit or base bias with one supply.



Base Bias

Base Bias with Emitter Feedback

This circuit is obtained by simply adding an emitter resistor to the base bias circuit as shown in Fig. below.



1. At saturation, V_{CE} is essentially zero; hence V_{CC} is distributed over R_L and R_E.

$$\therefore \qquad I_{C(sat)} = \frac{V_{CC}}{R_E + R_L}$$

2. I_C can be found as follows:

Consider the supply, base, emitter and ground route. Applying Kirchhoff's Voltage Law, we have

$$-I_B R_B - V_{BE} - I_E R_E + V_{CC} = 0$$

or $$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

Now $$I_B = I_C/\beta \quad \text{and} \quad I_E \cong I_C$$

Substituting these values in the above equation, we have

$$V_{CC} \cong \frac{I_C R_B}{\beta} + V_{BE} + I_C R_E$$

$$\therefore \qquad I_C \cong \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta} \cong \frac{V_{CC}}{R_E + R_B/\beta}$$ —neglecting VBE

3. Collector-to-ground voltage

$$V_C = V_{CC} - I_C R_L$$

4. Emitter-to-ground voltage

$$V_E = I_E R_E \cong I_C R_E$$

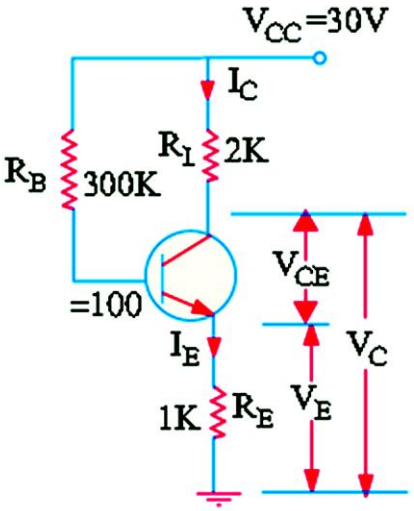
The β-sensitivity of this circuit is

$$K_\beta = \frac{1}{1 + \beta R_E / R_B}$$

Example: For the circuit shown in Fig. below, find (*i*) I_C (sat) , (*ii*) I_C , (*iii*) V_C , (*iv*) V_E, (*v*) V_{CE} and (*vi*) K_β.

Solution.

(*i*) $$I_{C(sat)} = \frac{V_{CC}}{R_E + R_L} = \frac{30}{1+2} = \mathbf{10\ mA}$$



(*ii*) $$\text{actual } I_C \cong \frac{V_{CC}}{R_E + R_B/\beta} = \frac{30}{1+300/100} = \mathbf{7.5\ m}$$

(*iii*) $$V_C = V_{CC} \times I_C R_L = 30 - 2 \times 7.5 = \mathbf{15\ V}$$

(*iv*) $$V_E \cong I_E R_E \cong I_C R_E = 7.5 \times 1 = \mathbf{7.5\ V}$$

(*v*) $$V_{CE} = V_C - V_E = 15 - 7.5 = \mathbf{7.5\ V}$$

(*vi*) $$K_\beta = \frac{1}{1+100\times 1/300} = \mathbf{0.75}$$

Base Bias with Collector Feedback

This circuit (Fig. below) is like the base bias circuit except that base resistor is returned to collector rather than to the V_{CC} supply. It derives its name from the fact that since voltage for R_B is derived from collector, there exists a negative feed-back effect which tends to stabilise I_C against changes in β. To understand this action, suppose that somehow β increases. It will increase I_C as well as I_C R_L but decrease V_C which is applied across R_B. Consequently, I_B will be decreased which will partially compensate for the original increase in β.

(i) $I_{C(sat)} = V_{CC}/R_L$ —since $V_{CE} = 0$

(ii) $V_C = V_{CC} - (I_B + I_C) R_L \cong V_{CC} - I_C R_L$

Also, $V_C = I_B R_B + V_{BE}$

Equating the two expressions for V_C, we have

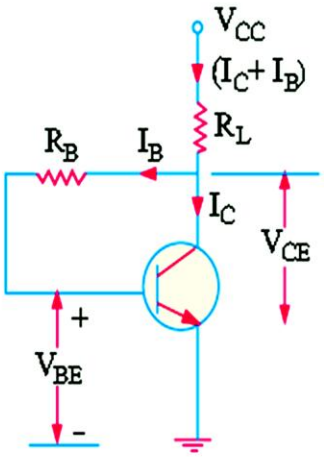
$I_B R_B + V_{BE} \cong V_{CC} \times I_C R_L$

Since $I_B = I_C/\beta$, we get

$$\frac{I_C}{\beta}.R_B + V_{BE} \cong V_{CC} - I_C R_L$$

$$\therefore \quad I_C = \frac{V_{CC} - V_{BE}}{R_L + R_B/\beta} \cong \frac{V_{CC}}{R_L + R_B/\beta}$$

$$K_\beta = \frac{1}{\beta R_L / R_B} = 1 - \frac{I_C}{I_{C(sat)}}$$



Base Bias with Collector and Emitter Feedbacks

In the circuit of Fig. below, both collector and emitter feedbacks have been used in an attempt to reduce circuit sensitivity to changes in β. If β increases, emitter voltage increases but collector voltage decreases. It means that voltage across R_B is reduced causing I_B to decrease thereby partially off-setting the increase in β. Under saturation conditions, V_{CC} is distributed over R_L and R_E. Assuming I_B to be negligible as compared to I_C, we get,

$I_{C(sat)} = V_{CC}/(R_E + R_L)$.

Actual value of I_C is $= \dfrac{V_{CC} - V_{BE}}{R_E + R_L + R_B/\beta}$

—going *via* R_B because V_{CE} is unknown.

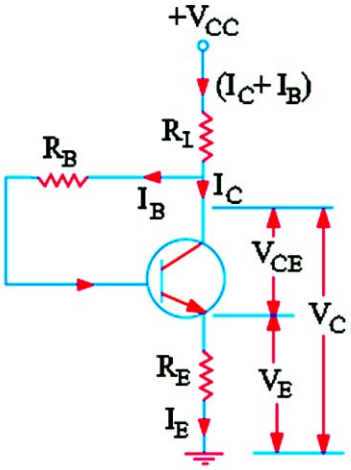
$V_C = V_{CC} - (I_C + I_B)$; $\quad R_L \cong V_{CC} - I_C R_L$

$V_E = I_E R_E \cong I_C R_E$; $\quad \overline{V}_{CE} = V_C - V_E$

$V_{CE} \cong V_{CC} - I_C (R_L + R_E)$

$$S = \frac{1 + R_B/(R_E + R_L)}{1 + R_B/\beta(R_E + R_L)}$$

It can be proved that $K_\beta = \dfrac{1}{1 + \beta(R_E + R_L)/R_B} = 1 - \dfrac{I_C}{I_{C(sat)}}$



Voltage Divider Bias

The name 'voltage divider' is derived from the fact that resistors R_1 and R_2 form a potential divider across V_{CC} (Fig. below). The voltage drop V_2 across R_2 forward-biases the emitter whereas V_{CC} supply reverse-biases the collector.

As per voltage divider theorem.

$$V_2 = V_{CC}.\, R_2/(R_1 + R_2)$$

As seen, $V_E = V_2 - V_{BE}$

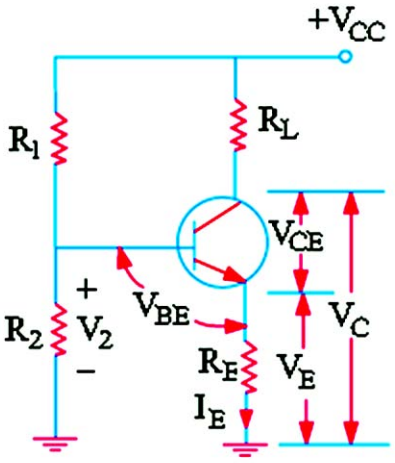
$$\therefore \quad I_E = \frac{V_E}{R_E} = \frac{V_2 - V_{BE}}{R_E} \cong \frac{V_2}{R_E}$$

Also, $V_C = V_{CC} - I_C R_L$

$$V_{CE} = V_C - V_E = V_{CC} - I_C R_L - I_E R_E$$
$$\cong V_{CC} - I_C(R_L + R_E) \quad \therefore \quad I_C \cong I_E$$

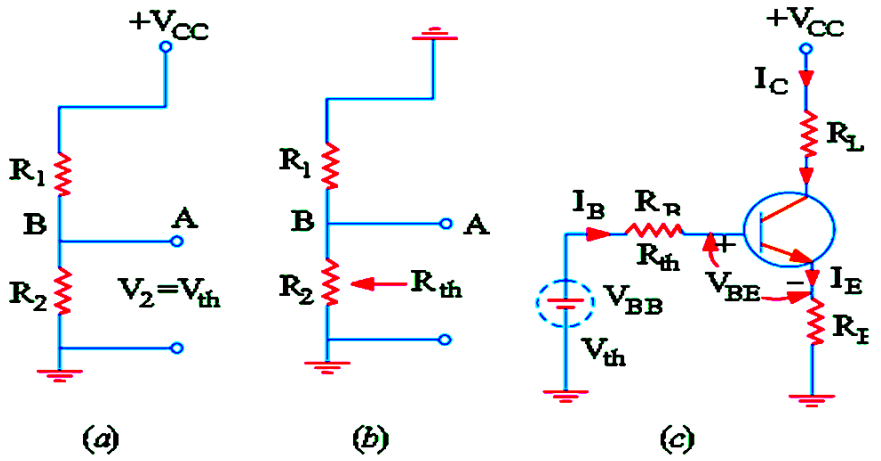
As before, $$I_{C(sat)} \cong \frac{V_{CC}}{R_L + R_E}$$

$$K_\beta = \frac{1}{1 + \beta R_E /(R_1 \| R_2)}$$



Using Thevenin's Theorem

More accurate results can be obtained by Thevenizing the voltage divider circuit as shown in Fig. below. The first step is to open the base lead at point A and remove the transistor along with R_L and R_E thereby leaving the voltage divider circuit behind as in (a) and (b).



$$V_{th} = V_2 = V_{CC} \cdot \frac{R_2}{R_1 + R_2} \quad \text{and} \quad R_{th} = R_1 \parallel R_2 = \frac{R_1 R_2}{(R_1 + R_2)}$$

The original circuit is reduced to that shown in Fig. (c) Where $V_{th}= V_{BB'}$; $R_{th}=R_{B'}$. Now, applying the β-rule to the circuit of fig.(b) we may find I_B and then $I_E=(1+\beta)I_B$ or we can find I_E directly.

$$I_B = \frac{V_{BB'} - V_{BE}}{R_{B'} + (1+\beta) R_E}$$

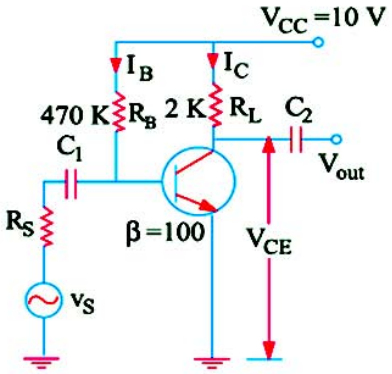
$$I_B = \frac{V_{BB'} - V_{BE}}{R_{B'} + \beta\ R_E}$$

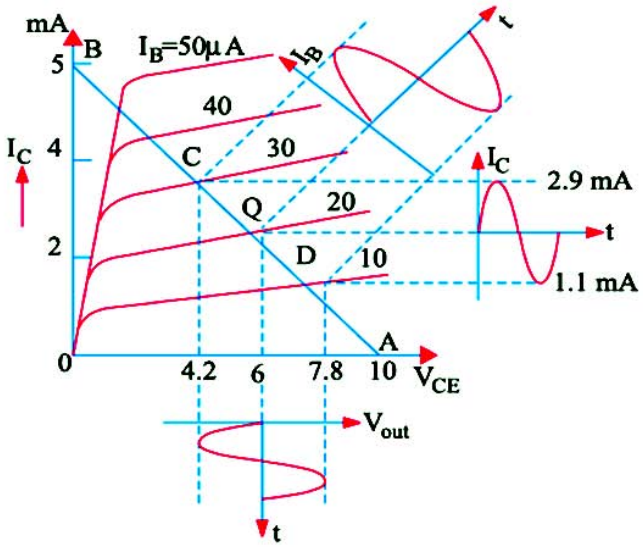
$$I_B = \frac{V_{BB'}}{R_{B'} + \beta\ R_E}$$

And $I_E=(1+\beta)I_B$

Load Line and Output Characteristics

Consider a silicon NPN transistor which is connected in CE configuration (Fig. below) and whose output characteristics are given in Fig. below. Let its β = 100. First, let us find the cut-off and saturation points for drawing the dc load line and then mark in the Q-point.





$I_{C(sat)} = 10/2 = 5$ mA —point B in Fig.

$V_{CE(cut\text{-}off)} = V_{CC} = 10$ V —point A in Fig.

Actual

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0.7}{470} = 20\,\mu A$$

$$I_C = \beta I_B = 100 \times 20 = 2000\ \mu A = 2\ mA$$

$$V_{CE} = V_{CC} \times I_C R_L = 10 - 2 \times 2 = 6\ V$$

This locates the *Q*-point in Fig. above.

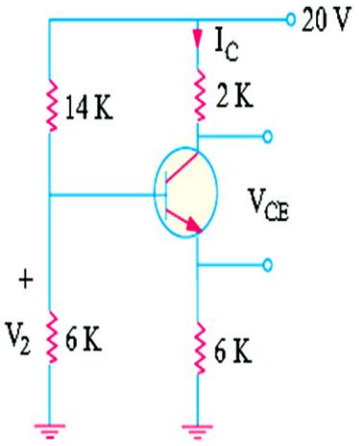
Also $$I_E = \frac{V_{BB}' - V_{BE}}{R_E + R_B'/(1+\beta)}$$

$$I_E = \frac{V_{BB}' - V_{BE}}{R_E \mid R_B'/(\beta)}$$

$$I_E = \frac{V_{BB}'}{R_E \mid R_B'/(\beta)}$$

$$V_{CE} = V_{CC} - I_C R_L - I_E R_E \cong V_{CC} - I_C(R_L + R_E)$$

Example. For the circuit of Fig. below, find (a) $I_{C(sat)}$, (b) I_C , (c) V_{CE} , (d) K_β. Neglect V_{BE} and take $\beta = 50$.



Solution.

(a) $I_{C(sat)} = \frac{V_{CC}}{R_L + R_E} = \frac{20}{2+6} =$ **2.5 mA**

(b) $I_C \cong I_E \cong V_2/R_E = 6/6 =$ **1 mA**

(c) $V_{CE} = V_{CC} - I_C(R_L + R_E) = 20 - 1\,(2+6) =$ **12 V**

(d) $R_1 \| R_2 = 84/20 = 4.2$ K

$$K_\beta = \frac{1}{1 + 50 \times 6/4.2} =$$ **0.0138**

Suppose an ac input signal voltage injects a sinusoidal base current of peak value 10 μA into the circuit of Fig. 1. It will swing the operating or *Q*-point up and down along the load line.

When positive half-cycle of I_B is applied, the *Q*-point shifts to point *C* which lies on the (20 + 10) = 30 mA line.

Similarly, during negative half-cycle of input base current, *Q*-point shifts to point *D* which lies on the (20 – 10) = 10 μA line.

By measurement, at point *C*, I_C = 2.9 mA. Hence, $V_{CE} = 10 - 2 \times 2.9 = 4.2$ V

Similarly, at point *D*, I_C measures 1.1 μA. Hence, $V_{CE} = 10 - 2 \times 1.1 = 7.8$ V

It is seen that V_{CE} decreases from 6 V to 4.2 V by a peak value of (6-4.2) = 1.8 V when base current goes positive. On the other hand, V_{CE} increases from 6 V to 7.8 V by a peak value of (7.8 – 6) = 1.8 V when input base current signal goes negative. Since changes in V_{CE} represent changes in output voltage, it means that when input signal is applied, I_B varies according to the signal amplitude and causes I_C to vary. It may e noted that variation in voltage drop across R_L are exactly the same as in V_{CE}.

Steady drop across R_L when no signal is applied =2*2=4V. When signal goes positive, drop across R_L=2*2.9=5.8V.when base signal goes negative I_C=1.1mA and drop across R_L= 2 × 1.1 = 2.2 V.

Hence, voltage variation is = 5.8 – 4 = 1.8 V during positive input half-cycle and 4 – 2.2 = 1.8 V during negative input half-cycle.

rms voltage variation $= 1.8/\sqrt{2} = 1.27V$.

Now, proper dissipated in R_L by ac component of output voltage is

$$P_{ac} = 1.27^2/2 = 0.81\ mW$$

$$P_{dc} = {I_C}^2 R_L = 2^2 \times 2 = 8mW$$

Total power dissipated in R_L=8.81mW.

AC Load Line

It is the line along which Q-point shifts up and down when changes in output voltage and current of an amplifier are caused by an ac signal.

This line is steeper than the dc line but the two intersect at the Q-point determined by biasing dc voltage and currents.

AC load line takes into account the ac load resistance whereas dc load line considers only the dc load resistance.

DC load line

The cut-off point for this line is where $V_{CE}=V_{CC}$. It is also written as V_{CE} (cut-off) saturation point is given by $I_C=V_{CC}/R_L$. It is represented by straight line AQB in Fig.1.

AC load line

The cut-off point is given by $V_{CE(cut\text{-}off)}=V_{CEQ}+I_{CQ}R_{ac}$,where R_{ac} is the ac load resistance. Saturation point is given by $I_{C(sat)}=I_{CQ}+V_{CEQ}/R_{ac}$.

It is represented by straight line CQD in Fig.1. The slope of the ac load line is given by $y=-1/R_{ac}$.

It is seen from Fig. 1 that maximum possible positive signal swing is = $I_{CQ}R_{ac}$. Similarly, maximum possible negative signal swing is V_{CEQ}.

Example: Draw the dc and ac load lines for the CE circuit shown in fig. below, (a) what is the maximum peak to peak signal that can be obtained?

Solution:

DC load line

$V_{CE(cut\text{-}off)}=V_{CC}=20V$. (point A)

$I_{C(Sat)}=V_{CC}/(R_L+R_E) = 20/5 = 4mA$ (point B).

Hence, AB represents dc load line for the given circuit.

Approximate bias conditions can be quickly found by assuming that I_B is too small to affect the base bias as in fig. below $V_2 = 20 \times 4/(4 + 16) = 4$ V. If we neglect V_{BE}, $V_2= V_E$;

$$I_E = \frac{V_E}{R_E} = \frac{V_2}{R_E} = \frac{4}{2} = 2\,\text{mA}$$

Also, $I_C \approx I_E = 2$ mA. Hence, $I_{CQ} = 2$ mA.

AC Load Line

Cut-off point, $V_{CE(cut\text{-}off)} = V_{CEQ} + I_{CQ}R_{ac}$

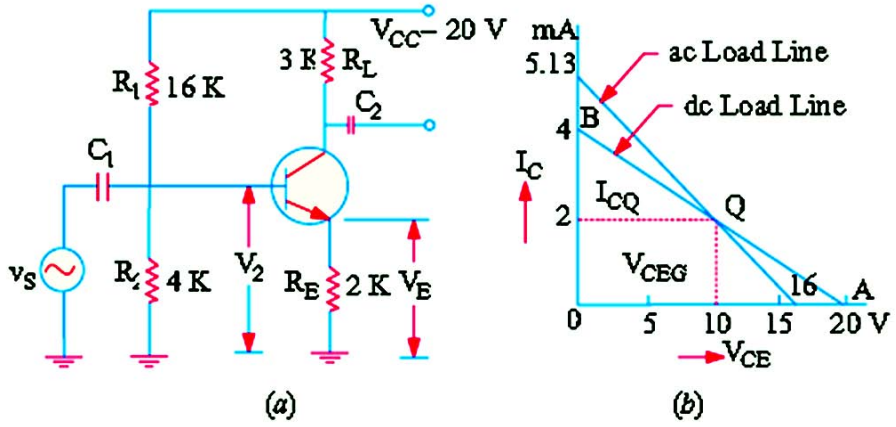
Now, for the given circuit, ac load resistance is $R_{ac} = R_C = 3K$.

Cut-off point = 10 + 2 × 3 = 16 V. Saturation point,

$$I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 2 + \frac{10}{3} = 5.13\,mA$$

Hence, line joining 16-V point and 5.13 mA. Point gives ac load line as shown in Fig. (b). As expected, this line passes through the Q-point.

Now, I_{CQ}. R_{ac} = 2 × 3 = 6 V and V_{CEQ}= 10 V. Taking the smaller quantity, maximum peak output signal = 6 V. Hence, peak-to-peak value = 2 × 6 = 12 V.



What are h-parameter?

These are four constants which describe the behavior of a two-port linear network. A linear network is one in which resistance, inductances and capacitances remain fixed when voltage across them is changed. Consider an unknown linear network contained in a black box as shown in Fig. 1. As a matter of convention, currents flowing into the box are taken positive whereas those flowing out of it are considered negative.

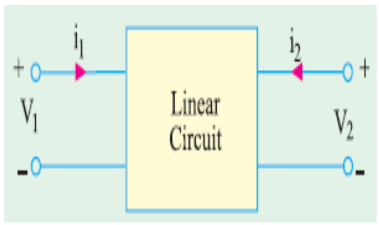


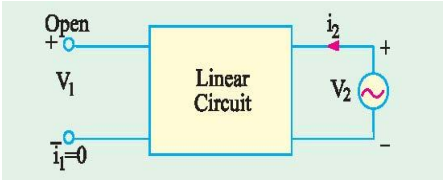
Fig.1

Similarly, voltages are positive from the upper to the lower terminals and negative the other way around. The electrical behavior of such a circuit can be described with the help of four hybrid parameters or constants designated as h_{ll}, h_{l2}, h_{2l}, h_{22}. In this type of double-number subscripts, it is implied that the first variable is always divided by the other. The subscript l refers to quantities on the input side and 2 to the quantities on the output side. The letter 'h' has come from the word hybrid which mixture of distinctly different items. These constants are hybrid because they have different units. Out of the four h-parameters, two are found by short-circuiting the output terminals 2-2 and the other two by open-circuiting the input terminals l-l of the circuit.

(a) Finding h_{ll} and h_{2l} from Short-Circuit Test

As shown in Fig. , the output terminals have been shorted so that $v_2 = 0$, because no voltage can exist on a short.

The linear circuit within the box is driven by an input voltage v_1. It produces an input current i_1 whose magnitude depends on the type of circuit within the box.



$$h_{11} \quad \frac{V_1}{i_2} \quad \text{— output shorted}$$

$$h_{21} \quad \frac{i_2}{i_1} \quad \text{— output shorted}$$

These two constants are known as forward parameters. The constant h_{11} represents input impedance with output shorted and has the unit of ohm. The constant h_{21} represents current gain of the circuit with output shorted and has no unit since it is the ratio of two similar quantities.

The voltages and currents of such a two-port network are related by the following sets of equations or V/I relations

$$V_1 = h_{11} i_1 + h_{12} V_2$$
$$i_2 = h_{21} i_1 + h_{22} V_2$$

Here, the hare constants for a given circuit but change if the circuit is changed. Knowledge of parameters enables us to find the voltages and currents with the help of the above two equations.

(b) Finding h_{12} and h_{22} from Open-circuit Test

As shown in Fig.3 , the input terminals are open so that $i_1 = 0$ but there does appear a voltage v_1 across them. The output terminals are driven by an ac voltage v_2 which sets up current i_2.

$$h_{12} \quad \frac{V_1}{V_2} \quad \text{— input open}$$

$$h_{22} \quad \frac{i_2}{V_2} \quad \text{— input open}$$

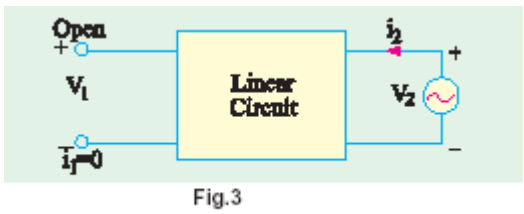


Fig.3

As seen, h_{12} represents voltage gain (not forward gain which is v_2 / v_1). Hence, it has no units. The constant h_{22} represents admittance (which is reverse of resistance) and has the unit of mho or Siemens, s.

It is actually the admittance looking into the output terminals with input terminals open. Generally, these two constants are also referred to as reverse parameters.

Summary of *h*-parameters

h_{11} =	input impedance	with output shorted
h_{21} =	forward current gain	
h_{12} =	reverse voltage gain	with input open
h =	output admittance	

The h-parameter Notation for Transistors

While using h-parameters for transistor circuits, their numerical subscripts are replaced by the first letters for defining them.

$h_{11} = h_i$ =	input impedance	output shorted
$h_{21} = h_f$ =	forward current gain	
$h_{12} = h_r$ =	reverse voltage gain	input open
$h_{22} = h_0$ =	output admittance	

A second subscript is added to the above parameters to indicate the particular configuration. For example, for CE connection, the four parameters are written as h_{ie}, h_{fe}, $h_{re,}$ h_{oe}. Similarly, for CB connection, these are written as h_{ib}, h_{fb}, h_{rb} and for CC connection as h_{ic}, h_{fc}, h_{rc} and h_{oc}

The h-parameters of an Ideal CB Transistor

A CB-connected transistor has been shown in Fig.4 (a), connected in a black box. Fig.4 (b) gives its equivalent circuit. It should be noted that no external biasing

resistors or any signal source has been shown connected to the transistor.

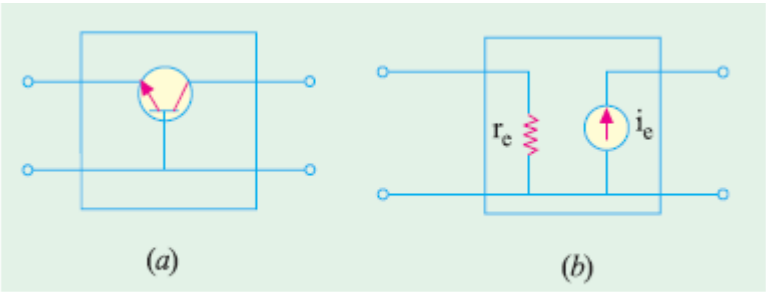


Fig. 4

(i) Forward Parameters

The two forward h-parameters can be found from the circuit of Fig.4 (a) where a short has been put across the output. The input impedance is simply r_e.

$$h_{ib} = r_e$$

The output current equals the input current i.e. Since it flows out of the box, it is taken as negative. The forward current gain is

$$h_{fb} \quad \frac{-i_e}{i_e} \quad 1$$

(It also called the ac α of the CB circuit.)

(ii) Reverse Parameters

The two reverse parameters can be found from the circuit diagram of Fig. (b). When input terminals are open, there can be no ac emitter current. It means that ac current source (inside the box) has a value of zero and so appears as an 'open'. Because of this open, no voltage can appear across input terminals, however, large V_2 may be. Hence, V_1=0.

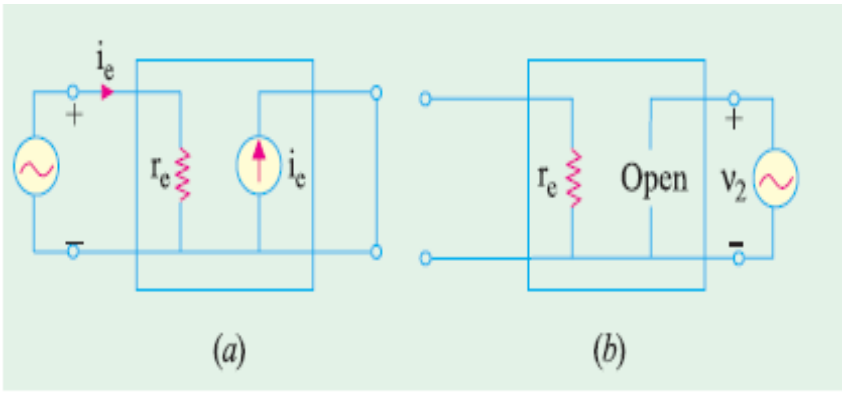


Fig.

$$\therefore \qquad h_{rb} \quad \frac{v_1}{v_2} \quad \frac{0}{v_2} \quad 0$$

Similarly, the impedance, looking into the output terminals is infinite. Consequently, its admittance (= l/∞) is zero.

$$\therefore \qquad h_{ob} = 0$$

The four h-parameters of an ideal transistor connected in CB configuration are;

$$h_{ib} = r_e \quad ; \qquad h_{fb} = -1, \quad h_{rb} = 0 \; ; \quad h_{ob} = 0$$

The equivalent hybrid circuit is shown in Fig. 5.

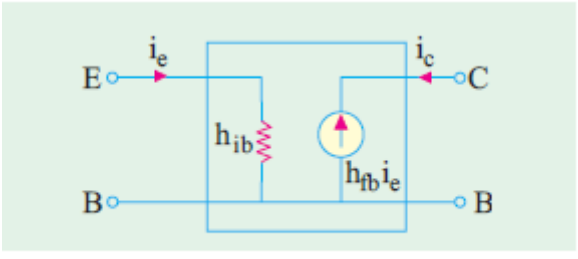


Fig. 5.

In reality, output impedance is not infinity but very high so that h_{ob} is extremely small. Similarly, there is some amount of feedback between the output and the input

circuits (even when open) though it is very small. Hence, h is very small.

The h--parameters of an ideal CE Transistor

Fig 6 (a) shows a CE-connected ideal transistor contained in a black box where shows its ac equivalent circuit in terms of its β and resistance values.

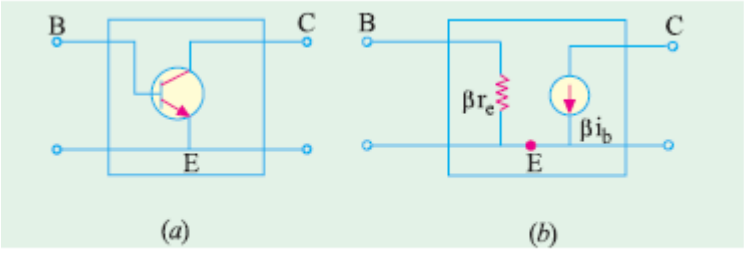


Fig. 6.

(a) Forward Parameters

The two forward h-parameters can be found from the circuit of Fig.7 (a)

Where output has been shorted. Obviously, the input impedance is simply βr_e

$$\therefore \qquad h_{ie}=\beta r_e$$

The forward current gain is given by

$$h_{fe} \quad \frac{i_2}{i_1} \quad \frac{i_b}{i_b}$$

(It is also called the ac beta of the CE circuit)

(b) Reverse Parameters

These can be found by reference to the circuit of Fig.7 (b), where input terminals are open but output terminals are driven by an are voltage source v_2 With input terminals open, there can be no base current so that i_b = o. If i_b= o, then collector current source has zero value i_b and looks like an open. Hence, there can be no v_1 due to this open.

$$\therefore \quad h_{re} \quad \frac{v_1}{v_2} \quad \frac{0}{v_2} \quad 0$$

Again, the impedance looking into the output terminals is infinite so that conductance is zero $\therefore \quad h_{oe} = 0$.

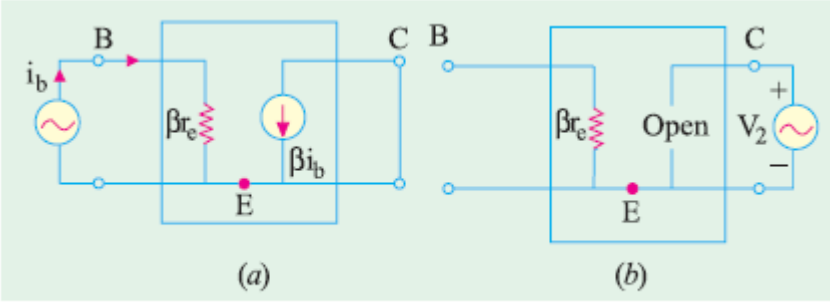


Fig. 7.

Hence, the four h-parameters of an ideal transistor connected in CE transistor are

$$h_{ie} = \beta r_e; \quad h_{fe} = \beta, \quad hr_e = 0; \quad h_{oe} = 0.$$

The hybrid equivalent circuit of such transistor is shown in fig.8.

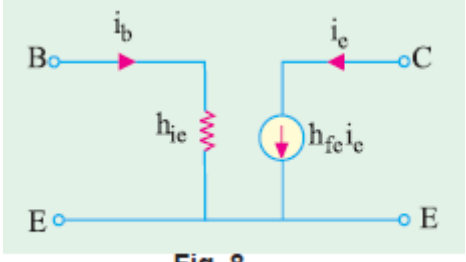


Fig. 8

Approximate Hybrid Equivalent Circuits

(a) Hybrid CB Circuit

In Fig. 9. (a) is shown an NPN transistor connected in CB configuration. Its ac equivalent circuit employing h-parameters is shown in Fig. 9 (b).

The V/I relationships are given by the following two equations

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb}$$
$$i_e = h_{fb} i_e + h_{ob} v_{eb}$$

These equations are self-evident because applied voltage across input terminals must equal the drop over h_{ib} and the generator voltage. Similarly, current i_c the output terminals must equal the sum of two branch currents.

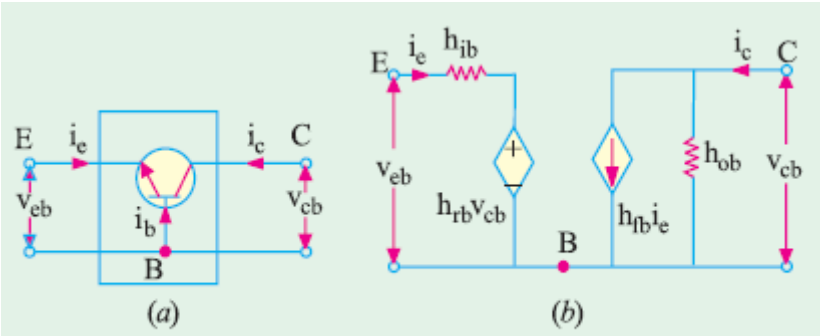


Fig. 9

(b) Hybrid CE Circuit

The hybrid equivalent of the transistor alone when connected in CE configuration is shown in Fig.10 (b). Its V/I characteristics are described by the following two equations.

$$v_{be} = h_{ie} i_b + h_{re} v_{ec}$$
$$i_e = h_{fb} i_b + h_{oe} v_{ec}$$

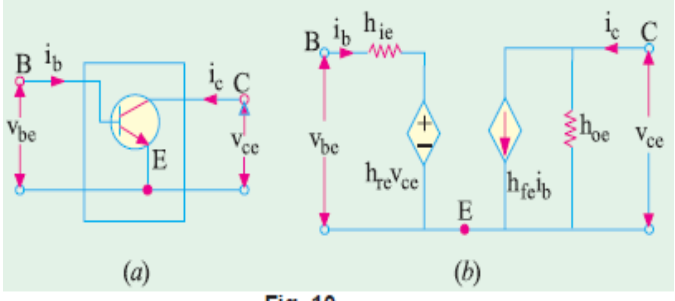


Fig. 10.

(c) Hybrid CC Circuit

The hybrid equivalent of a transistor alone when connected in CC Configuration is shown in Fig.11(b). Its V/I characteristics are defined by the following two equations :

$$V_{be} = h_{ie} i_b + h_{re} V_{ec}$$
$$i_e = h_{fe} i_b + h_{oc} V_{ce}$$

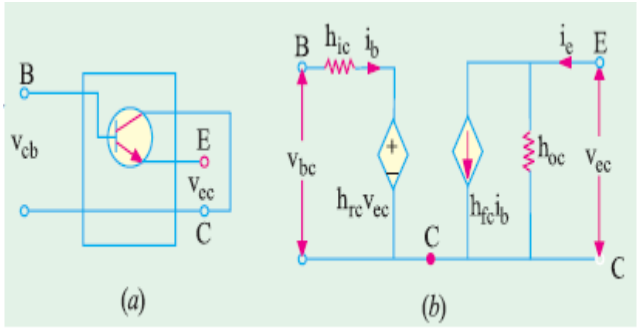


Fig. 11

We may connect signal input source across output terminals BC and load resistance across output terminals EC to get a CC amplifier.

Typical Values of Transistor h-parameters

In the table below are given typical values for each parameter for the broad range of transistors available today in each of the three configurations.

Parameter	*CB*	*CE*	*CC*
h_i	25 Ω	1 K	1 K
h_r	3×10^{-4}	2.5×10^{-4}	≅ 1
h_f	–0.98	50	–50
h_o	0.5×10^{-6}S	25×10^{-6}S	25×10^{-6}S

Approximate Hybrid Formulas

The approximate hybrid formulas for the three connections are listed below. These are applicable when h_o and h_r is very small and R_s is very large. The given values refer to transistor terminals. The values of $r_{in(stage)}$ or r_{in} and $r_{o(stage)}$ will depend on biasing resistors and load resistance respectively.

Item	CE	CB	CC
r_{in}	h_{ie}	h_{ib}	$h_{ic} + h_{fe}R_L$
r_o	$\frac{1}{h_{oc}}$	$\frac{1}{h_{oB}}$	$\frac{h_{ie}}{h_{fc}}$
A_i	$h_{fe} = \beta$	$-h_{fb} \cong 1$	$-h_{fe} \cong \beta$
A_v	$\frac{h_{ie}R_C}{h_{is}}$	$\frac{f_{fb}}{h_{ib}}R_C$	1

Common Emitter h-parameter Analysis

The h-parameter equivalent of the CE circuit of Fig.12 , no emitter resistor has been connected.

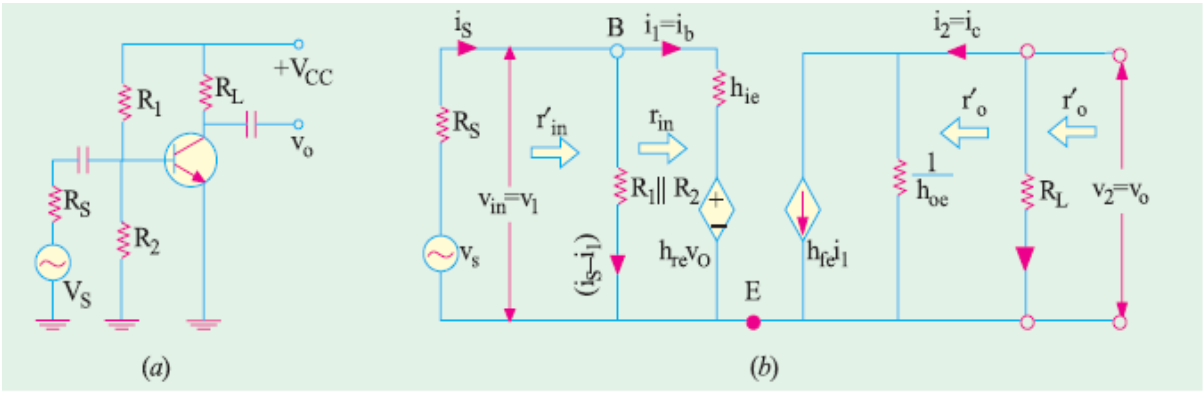


Fig. 12

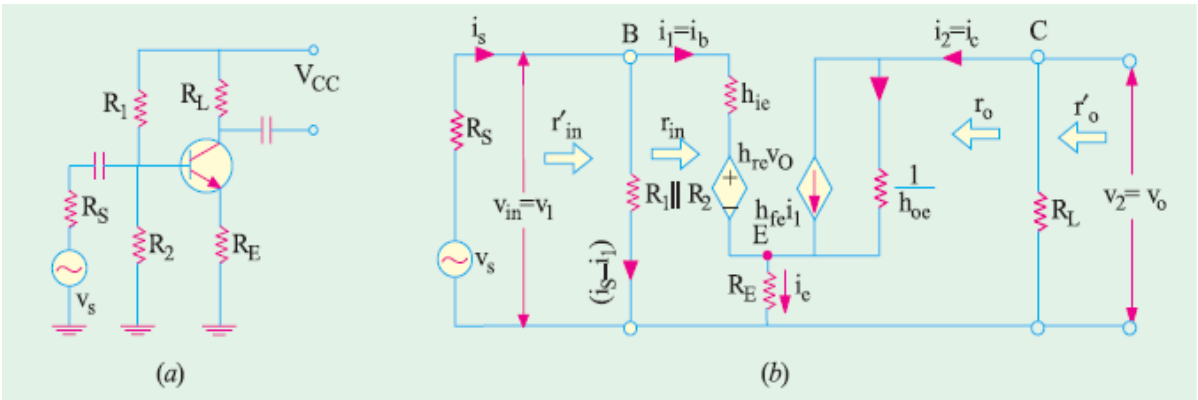


Fig. 13

We will now derive expressions for voltage and current gains for both these circuits.

l. Input Impedance

When looking into the base-emitter terminals of the transistor, h_{ie} in series with h_{re} no. For a CE circuit, h_{re} is very small so that h_{re} V_o is negligible as compared to the drop over h_{ie}. Hence, $r_{in}=h_{ie}$.

Now, consider the circuit of Fig.13. Again ignoring h_{re} V_o we have

$$v_1 = h_{ie} i_b + i_e R_E = h_{ie} i_b + (i_b + i) R_E$$
$$= h_{ie} i_b + i_b R_E + h_{fe} i_b R_E \qquad ((\quad i_c \quad h_{fe} i_b)$$
$$= i_b [h_{ie} + R_E (1 + h_{fe})]$$

$$\therefore \qquad r_{in} = r_{in(base)} = \frac{v_1}{i_1} \quad \frac{v_1}{i_b} \quad h_{ie} \quad (1 \quad h_{fe}) R_E \ *$$

$$r_{in} \text{ or } r_{in(base)} = R_1 \,||\, R_2 \,||\, r_{in(base)}$$

2. Output Impedance

Looking back into the collector and emitter terminals of the transistor in Fig. (12 b), $r_o = 1/h_{oe}$.

As seen, r_o' or $r_{o(stage)} = r_o \,||\, R_L = (1/h_o) \,||\, r_L \qquad (\quad r_L \quad R_L)$
Since $1/h_{oe}$ is typically 1 M or so and R_L is usually much smaller, $r_o' \cong R_L = r_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $v_o = - i_c R_L$ and $v_{in} \cong i_b h_{ie}$

$$\therefore \quad A_v \quad \frac{i_s R_L}{i_b h_{ie}} \quad \frac{i_c}{i_b} \cdot \frac{R_L}{h_{ie}} \quad \frac{h_f R_L}{h_{ie}}$$

Now, consider Fig.13(b). Ignoring $h_{re} v_o$, we have from the input loop of the circuit

$$v_{in} = i_b [h_{ie} + R_E (1 + h_{fe})] \qquad \text{–proved above}$$

$$\therefore \quad A_v \quad \frac{v_o}{v_{in}} \quad \frac{i_c R_L}{i_b [h_{ie} \quad R_E (1 \quad h_{fe})]} \quad \frac{h_{fe} R_L}{h_{fe} \quad (1 \quad h_{fe}) R_E}$$

$$\frac{R_L}{R_E} \qquad \text{— if } (1 + h_{fe}) R_E >> h_{ie}$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{h_{fe}}{1 \quad h_{oe} r_L} \quad h_{fe} \qquad \text{— if } h_{oe} r_L << 1$$

$$A_{is} \quad \frac{h_{fe} \cdot R_1 \| R_2}{r_{in} \quad R_1 \| R_2}$$

5. Power Gain

$$A_p = A_v \times A_i$$

Common Collector h-parameter Analysis

The CC transistor circuit and its h-parameter equivalent are shown in Fig.14

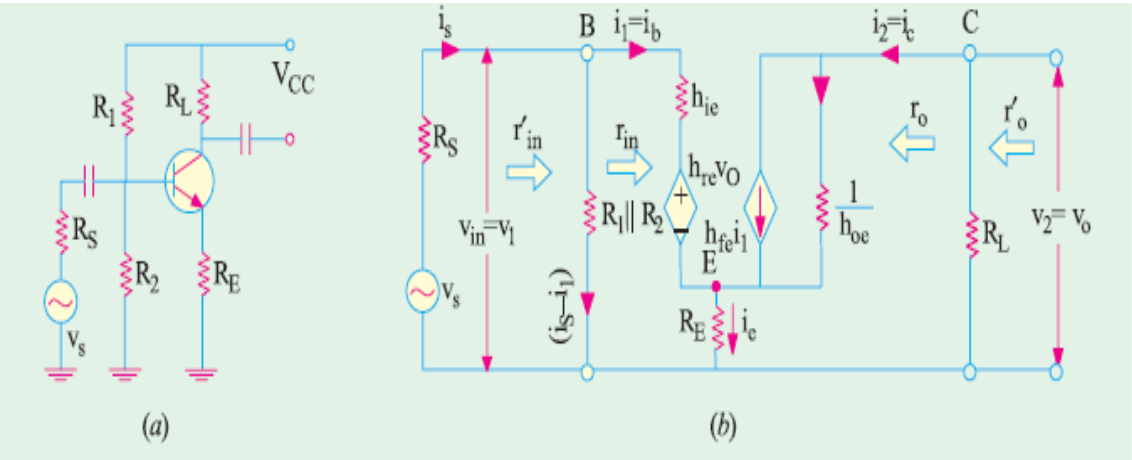


Fig.14

l. Input Impedance

$$v_{in} = i_b h_{ic} + h_{rc} v_o = i_b h_{ic} + v_o = i_b h_{ic} + i_e R_L$$
$$= i_b h_{ic} + h_{fe} i_b R_L = i_b (h_{ic} + h_{fe} R_L) \qquad i_c = h_{fe} i_b$$

$$\therefore \qquad r_{in} \quad \frac{v_{in}}{i_b} \quad h_{ic} \quad h_{fe} R_L$$

As seen, $r_{in(stage)} = r_{in(base)} \| R_1 \| R_2 = r_{in(base)} \| R_B$ where $R_B = R_1 \| R_2$

2. Output Impedance

$$r_o \quad \frac{v_2}{i_2}\Big|_{v_s\ 0} \qquad \frac{v_o}{i_c}\Big|_{v_s\ 0}$$

Now, $i_e \cong i_c = h_{fe} i_b = h_{fc} i_1$

Since $v_s = 0$, i_b is produced by $h_{rc} v_o = v_o$

Hence, considering the input circuit loop, we get

$$i_b \quad \frac{v_0}{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)} \quad \frac{v_0}{h_{ic} \quad R_S \parallel R_B}$$

$$i_c \quad h_{fc} i_b \quad \frac{h_{fc} v_o}{h_{ic} \quad (R_S \parallel R_B)} \qquad \text{where } R_B = R_1 \parallel R_2$$

$$\therefore \qquad r_o \quad \frac{V_o}{i_e} \quad \frac{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)}{h_{fe}}$$

Also, r_o' or $r_{o(stage)} = r_o \parallel R_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $v_o = i_e R_L = h_{fe} i_b R_L$ and $i_b = (v_{in} - v_o) / h_{ic}$

$$v_o \quad \frac{h_{fe} R_L}{h_{ie}} (v_{in} \quad v_o) \quad \text{or} \quad v_o \ 1 \quad \frac{h_{fe} R_L}{h_{ic}} \quad \frac{h_{fe} R_L v_{in}}{h_{ic}}$$

$$\therefore \qquad A_v \quad \frac{v_o}{v_{in}} \quad \frac{h_{fe} R_L / h_{ic}}{1 \quad h_{fe} R_L / h_{ic}} \quad 1$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{i_e}{i_b} \quad h_{fe}\ ; \ A_{is} \quad \frac{h_{fe} R_B}{r_{in} \quad R_B} \qquad \text{where } R_B = R_1 \parallel R_2$$

Conversion of h-parameters

Transistor data sheets generally specify the transistor in terms of its h-parameters for CB connection i.e. h_{ib}, h_{fb}, h_{rb} and h_{ob}. If we want to use the transistor in CE or CC configuration we will have to convert the given set of parameters into a set of CE or CC parameters. Approximate conversion formulae are tabulated over leaf :

Table

From CB to CE	*From CE to CB*	*From CE to CC*
$h_{ie} \quad \frac{h_{ib}}{1 \quad h_{fb}}$	$h_{ie} \quad \frac{h_{ie}}{1 \quad h_{fe}}$	$h_{ic} = h_{ic}$
$h_{oe} \quad \frac{h_{ob}}{1 \quad h_{fb}}$	$h_{ob} \quad \frac{h_{oe}}{1 \quad h_{fe}}$	$h_{oc} = h_{oe}$
$h_{fe} \quad \frac{h_{fb}}{1 \quad h_{fb}}$	$h_{fb} \quad \frac{h_{fe}}{1 \quad h_{fe}}$	$h_{fe} = -(1 + h_{fe})$
$h_{re} \quad \frac{h_{ib} h_{ob}}{1 \quad h_{fb}} \quad h_{rb}$	$h_{rb} \quad \frac{h_{ie} h_{oe}}{1 \quad h_{fe}} \quad h_{re}$	$h_{re} = 1 - h_{re} \cong 1$

Example. *A transistor used in CB circuit has the following set of parameters.*

$h_{ib} = 36\ \Omega, h_{fb} = 0.98, h_{rb} = 5 \times 10^{-4}, h_{ob} = 10^{-6}$ *Siemens*

With $R_S = 2$ *K and* $R_C = 10$ *K, calculate* (*i*) $r_{in(base)}$ (*ii*) r_{out} (*iii*) A_i and (*iv*) A_v.

Solution. Approximate Values

(*i*) $r_{in} = h_{ib} = 36\ \Omega$ (*ii*) $r_o \quad \frac{1}{h_{ob}} \quad \frac{1}{10^{-6}} \quad 1\text{M}$

(*iii*) $A_i = h_{fb} = -0.98$ (*iv*) $A_v \quad \frac{h_{fb}}{h_{ib}} \quad R_C \quad \frac{0.98}{36} \quad 10\text{K} \quad 272$

More Accurate Values

(*i*) $r_{in(base)} \quad h_{ib} \quad \frac{h_{rb} h_{fb}}{h_{ob} \quad 1/r_L}$

$= 36 \quad \frac{0.98 \quad 5 \quad 10^{-4}}{10^{-6} \quad 1/10 \quad 10^3}$ ($\therefore \quad r_L = R_C$ since there is no R_L)

$= 36 + 4.9 = 40.9\ \Omega$

It is the input resistance at transistor terminals.

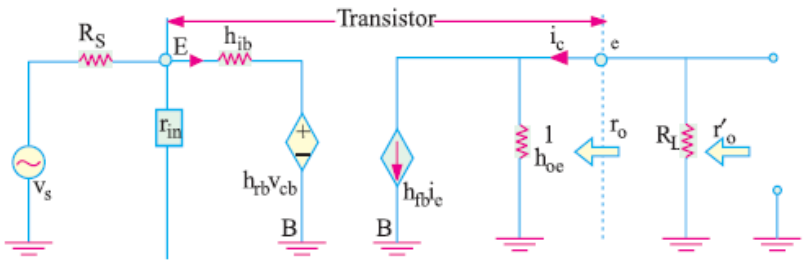


Fig. 15

(*ii*) $r_o \quad \frac{h_{ib} \quad R_s}{h_o (h_{ib} \quad R_S) \quad h_{fb} . h_{rb}} \quad \frac{36 \quad 2000}{10^{-6} (36 \quad 2000) \quad (0.98) \quad 5 \quad 10^{-4}} \quad 0.8\ \text{M}$

It is the output resistance at transistor terminals.

(*iii*) $A_i \quad \frac{h_{fb}}{1 \quad h_{ob} r_L} \quad \frac{0.98}{1 \quad 10^{-6} \quad 10^4} \quad -0.97$

(*iv*) $A_v \quad \frac{h_{fb} r_L}{h_{ib} (1 \quad h_{ob} r_L) \quad h_{fb} h_{rb} . r_L}$ ($r_L \quad R_L$)

Here, ac load $r_L = R_L = 10\ \text{K} = 104\ \Omega$

$\therefore \quad A_v \quad \frac{(0.98) \quad 10^4}{36 (1 \quad 10^{-6} \quad 10^4) \quad (0.98) \quad 5 \quad 10^{-4} \quad 10^4} \quad 249$

Example *A transistor used in CE connection has the following set of h-parameters : $h_{ir} = 1$ K, $h_{fe} = 100$, $h_{re} = 5 \times 10^{-4}$ and $h_{oc} = 2 \times 10^{-5}$ S. With $R_S = 2$ K and $R_C = 5$ K, determine*

(i) r_{in} (ii) r_o (iii) A_i and (iv) A_v

Solution.

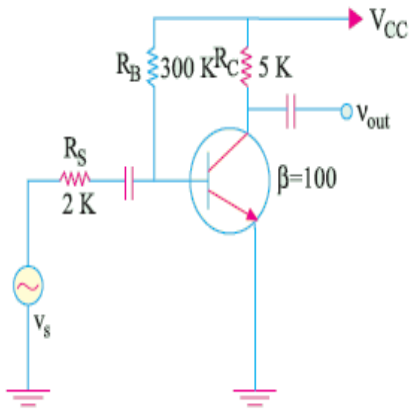


Fig. 16

(i) $r_{in} \quad h_{ie} \quad \dfrac{h_{fb} r_L}{h_o \quad 1/r_L}$

$= 1000 \quad \dfrac{5 \quad 10^{4} \quad 100}{2 \quad 10^{5} \quad 1/5 \quad 10^{3}}$

$= 723\ \Omega$

(ii) $r_o \quad \dfrac{h_{ie} \quad R_s}{(h_{ie} \quad R_s) h_{oe} \quad h_{fe} . h_{re}} \quad \dfrac{1000 \quad 2000}{(1000 \quad 2000) \quad 10^{5} \quad 100 \quad 5 \quad 10^{4}}$

$= 30{,}000\Omega = 0.03$ M

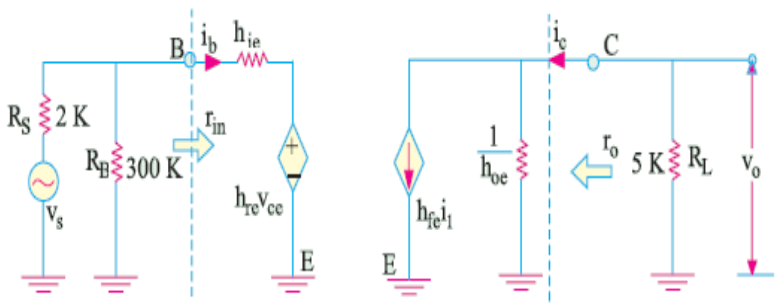


Fig. 17

(iii) $A_i \quad \dfrac{h_{fe}}{1 \quad h_{oe} r_L} \quad \dfrac{100}{1 \quad 2 \quad 10^{5} \quad 5 \quad 10^{3}} \quad 91$

(iv) $A_i \quad \dfrac{h_{fe} r_L}{(h_{ie} \quad R_s)(1 \quad h_{oe} . r_L) \quad h_{fe} h_{re} r_L}$

$$\frac{100 \quad 5 \quad 10^{3}}{(100 \quad 2000)(1 \quad 2 \quad 10^{5} \quad 5 \quad 10^{3}) \quad 100 \quad 5 \quad 10^{4} \quad 5 \quad 10^{3}} \quad -164$$

The negative sign indicates that there is 180° phase shift between the input and output ac signals. Obviously, it is the overall (or circuit) voltage gain and not the voltage gain of the transistor alone.

Example *The transistor of Fig. has the following set of h-parameters :*

$h_{ie} = 2\ \text{K}, h_{fe} = 100, h_{re} = 5 \times 10^{-4}, h_{oe} = 2.5 \times 10^{-5}\ \text{S}$

Find the voltage gain and the ac impedance of the stage.

Solution. Using somewhat exact formul

$$r_{in(base)} \quad h_{ie} \quad \frac{h_{fe}h_{re}}{h_{oe} \quad 1/r_L}$$

Now, collector load

$$r_L = 10\ \text{K} \parallel 30\ \text{K} = 7.5\ \text{K}$$

$$\therefore \quad r_{in(base)} \quad 200 \quad \frac{100 \quad 5 \quad 10^{4}}{2.5 \quad 10^{5} \quad 1/7.5 \quad 10^{3}}$$

$$= 2000 - 316 = \mathbf{1684\ \Omega}$$

The ac input impedance of the stage *i.e.* impedance when looking into point *B* is

$$r_{in(base)} = r_{in(base)} \parallel R_1 \parallel R_2 = 1.684 \parallel 50 \parallel 25 = \mathbf{1.53K}$$

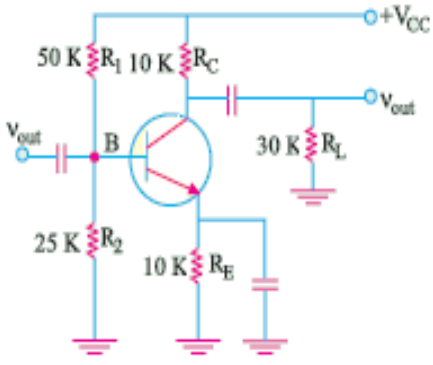


Fig.

$$A_v \quad \frac{h_{fe}}{r_{in(base)}(h_{oe} \quad 1/r_L)} \qquad \text{Now,} \quad r_L = 10\ \text{K} \parallel 30\ \text{K} = 7.5\ \text{K}$$

$$\therefore \quad A_v \quad \frac{100}{0184\ (2.5 \quad 10^{5} \quad 1/7500)} \quad \mathbf{-375}$$

Obviously, R_E does not come into the ac picture because it is ac grounded by the bypass capacitor.

Example *In the CC circuit of Fig. the transistor parameter are $h_{ie} = 2K$ and $h_{fe} = 100$. Calculate the circuit input and output impedance and voltage, current and power gains.*

Solution. $r_{in} \cong h_{ie} + h_{fe} R_L = 2 + 100 \times 5 = \mathbf{502\ K}$

$$r_{in(stage)} = R_1 \parallel R_2 \parallel r_{in}$$

$$= 10 \parallel 10 \parallel 502 = \mathbf{4.95\ K}$$

$$r_o \quad \frac{h_{ie} \quad (R_s \parallel R_1 \parallel R_2)}{h_{fe}}$$

$$\frac{2 \quad (1 \parallel 10 \parallel 100)}{100} \quad \mathbf{28.3\ \Omega}$$

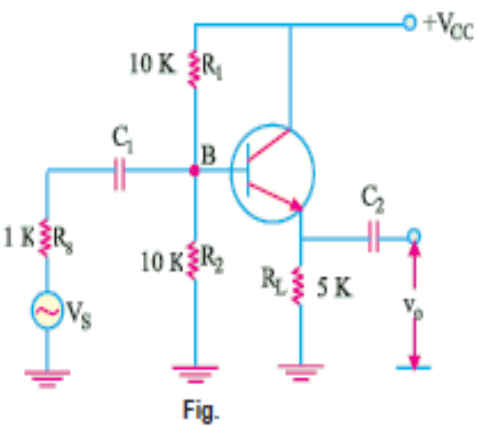


Fig.

$$r_{o(stage)} = r_o \parallel R_L = 28.3\ \Omega \parallel 5\text{K}$$

$$= \mathbf{28.1\Omega}$$

$$A_v \cong 1 \text{ and } A_i = h_{fe} = 100$$

1.What is an OP-AMP ?

It is a very high-gain, amplifier which can amplify signals having frequency ranging from **0 Hz to a little beyond 1 MHz.** They are made with different internal configurations in linear *ICs*. An *OP-AMP* is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation and integration etc. in analog computers. Present day usage is much wider in scope but the popular name *OP-AMP* continues.

Although an *OP-AMP* is a complete amplifier, it is so designed that external components (resistors, capacitors etc.) can be connected to its terminals to change its external characteristics. Hence, it is relatively easy to tailor this amplifier to fit a particular application and it is, in fact, due to this versatility that *OP-AMPs* have become so popular in industry.

2. OP-AMP Symbol

Standard triangular symbol for an *OP-AMP* is shown in Fig.1 (*a*) though the one shown in Fig.1 (*b*) is also used often. In Fig.1 (*b*), **the common ground line has been omitted.** It also does not show other necessary connections such as for dc power and feedback etc. The *OP-AMP's* input can be single ended or double-ended (or differential input) depending on whether input voltage is applied to one input terminal only or to both. Similarly, amplifier's output can also be either single-ended or double ended.

The most common configuration is ***two input terminals and a single output.***

All OP-AMPs have a minimum of five terminals :

1. inverting input terminal, **2.** non-inverting input terminal,

3. output terminal, **4.** positive bias supply terminal,

$$\therefore \quad h_{re} \quad \frac{v_1}{v_2} \quad \frac{0}{v_2} \quad 0$$

Again, the impedance looking into the output terminals is infinite so that conductance is zero $\therefore \quad h_{oe} = 0$.

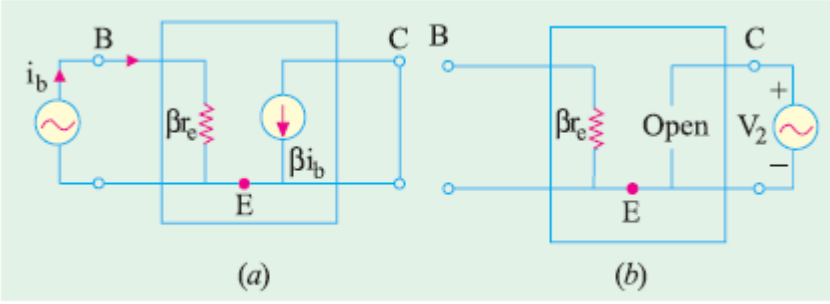


Fig. 7.

Hence, the four h-parameters of an ideal transistor connected in CE transistor are

$$h_{ie} = \beta r_e; \quad h_{fe} = \beta, \quad hr_e = 0; \quad h_{oe} = 0.$$

The hybrid equivalent circuit of such transistor is shown in fig.8.

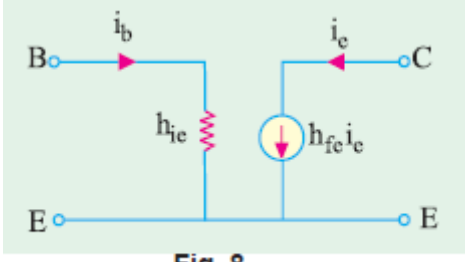


Fig. 8

Approximate Hybrid Equivalent Circuits

(a) Hybrid CB Circuit

In Fig. 9. (a) is shown an NPN transistor connected in CB configuration. Its ac equivalent circuit employing h-parameters is shown in Fig. 9 (b).

The V/I relationships are given by the following two equations

$$v_{eb} = h_{ib} i_e + h_{rb} v_{cb}$$
$$i_e = h_{fb} i_e + h_{ob} v_{eb}$$

These equations are self-evident because applied voltage across input terminals must equal the drop over h_{ib} and the generator voltage. Similarly, current i_c the output terminals must equal the sum of two branch currents.

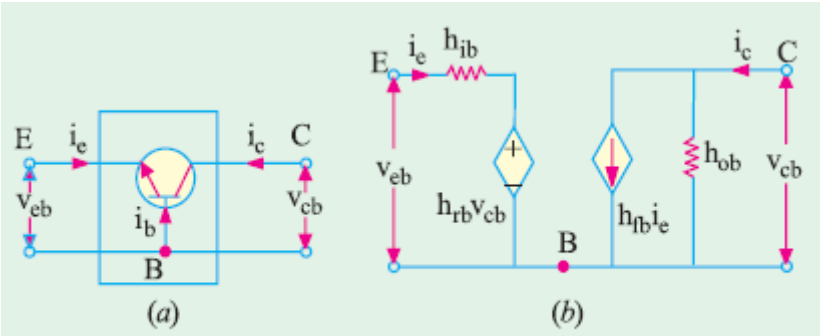


Fig. 9

(b) Hybrid CE Circuit

The hybrid equivalent of the transistor alone when connected in CE configuration is shown in Fig.10 (b). Its V/I characteristics are described by the following two equations.

$$v_{be} = h_{ie} i_b + h_{re} v_{ec}$$
$$i_e = h_{fb} i_b + h_{oe} v_{ec}$$

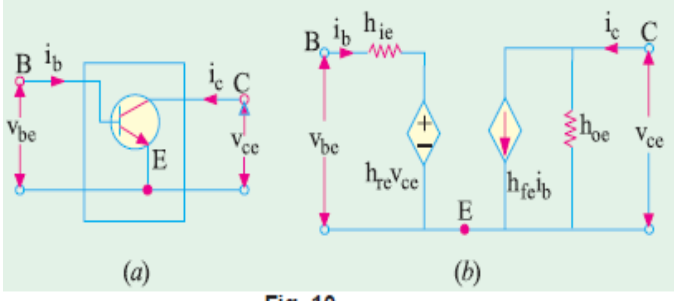


Fig. 10.

(c) Hybrid CC Circuit

The hybrid equivalent of a transistor alone when connected in CC Configuration is shown in Fig.11(b). Its V/I characteristics are defined by the following two equations :

$$V_{be} = h_{ie} i_b + h_{re} V_{ec}$$
$$i_e = h_{fe} i_b + h_{oc} V_{ce}$$

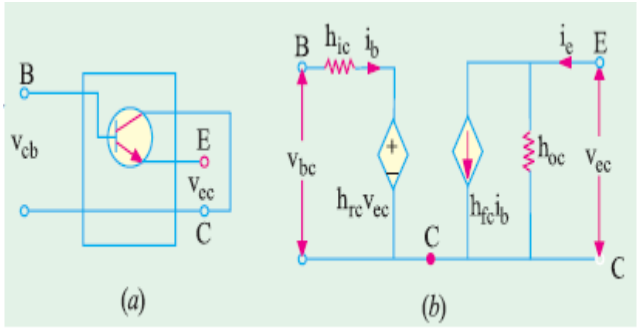


Fig. 11

We may connect signal input source across output terminals BC and load resistance across output terminals EC to get a CC amplifier.

Typical Values of Transistor h-parameters

In the table below are given typical values for each parameter for the broad range of transistors available today in each of the three configurations.

Parameter	*CB*	*CE*	*CC*
h_i	25 Ω	1 K	1 K
h_r	3×10^{-4}	2.5×10^{-4}	≅ 1
h_f	–0.98	50	–50
h_o	0.5×10^{-6}S	25×10^{-6}S	25×10^{-6}S

Approximate Hybrid Formulas

The approximate hybrid formulas for the three connections are listed below. These are applicable when h_o and h_r is very small and R_s is very large. The given values refer to transistor terminals. The values of $r_{in(stage)}$ or r_{in} and $r_{o(stage)}$ will depend on biasing resistors and load resistance respectively.

Item	CE	CB	CC
r_{in}	h_{ie}	h_{ib}	$h_{ic} + h_{fe}R_L$
r_o	$\frac{1}{h_{oc}}$	$\frac{1}{h_{oB}}$	$\frac{h_{ie}}{h_{fc}}$
A_i	$h_{fe} = \beta$	$-h_{fb} \cong 1$	$-h_{fe} \cong \beta$
A_v	$\frac{h_{ie}R_C}{h_{is}}$	$\frac{f_{fb}}{h_{ib}}R_C$	1

Common Emitter h-parameter Analysis

The h-parameter equivalent of the CE circuit of Fig.12 , no emitter resistor has been connected.

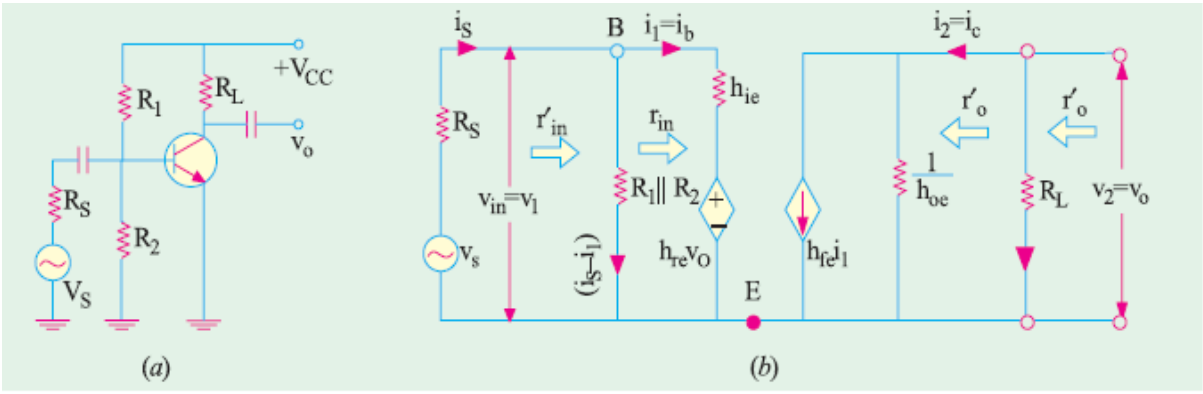


Fig. 12

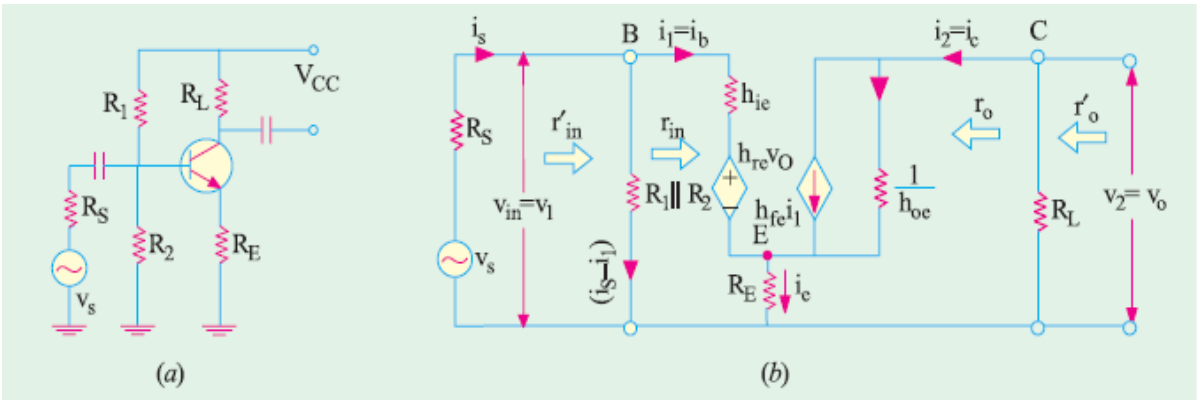


Fig. 13

We will now derive expressions for voltage and current gains for both these circuits.

l. Input Impedance

When looking into the base-emitter terminals of the transistor, h_{ie} in series with h_{re} no. For a CE circuit, h_{re} is very small so that h_{re} V_o is negligible as compared to the drop over h_{ie}. Hence, $r_{in}=h_{ie}$.

Now, consider the circuit of Fig.13. Again ignoring h_{re} V_o we have

$$v_1 = h_{ie} i_b + i_e R_E = h_{ie} i_b + (i_b + i) R_E$$
$$= h_{ie} i_b + i_b R_E + h_{fe} i_b R_E \qquad ((\quad i_c \quad h_{fe} i_b)$$
$$= i_b [h_{ie} + R_E (1 + h_{fe})]$$

$$\therefore \qquad r_{in} = r_{in(base)} = \frac{v_1}{i_1} \quad \frac{v_1}{i_b} \quad h_{ie} \quad (1 \quad h_{fe}) R_E \ *$$

$$r_{in} \text{ or } r_{in(base)} = R_1 \,||\, R_2 \,||\, r_{in(base)}$$

2. Output Impedance

Looking back into the collector and emitter terminals of the transistor in Fig. (12 b), $r_o = 1/h_{oe}$.

As seen, r_o' or $r_{o(stage)} = r_o \,||\, R_L = (1/h_o) \,||\, r_L \qquad (\quad r_L \quad R_L)$
Since $1/h_{oe}$ is typically 1 M or so and R_L is usually much smaller, $r_o' \cong R_L = r_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $v_o = - i_c R_L$ and $v_{in} \cong i_b h_{ie}$

$$\therefore \quad A_v \quad \frac{i_s R_L}{i_b h_{ie}} \quad \frac{i_c}{i_b} \cdot \frac{R_L}{h_{ie}} \quad \frac{h_f R_L}{h_{ie}}$$

Now, consider Fig.13(b). Ignoring $h_{re} v_o$, we have from the input loop of the circuit

$$v_{in} = i_b [h_{ie} + R_E (1 + h_{fe})] \qquad \text{–proved above}$$

$$\therefore \quad A_v \quad \frac{v_o}{v_{in}} \quad \frac{i_c R_L}{i_b [h_{ie} \quad R_E (1 \quad h_{fe})]} \quad \frac{h_{fe} R_L}{h_{fe} \quad (1 \quad h_{fe}) R_E}$$

$$\frac{R_L}{R_E} \qquad \text{— if } (1 + h_{fe}) R_E >> h_{ie}$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{h_{fe}}{1 \quad h_{oe} r_L} \quad h_{fe} \qquad \text{— if } h_{oe} r_L << 1$$

$$A_{is} \quad \frac{h_{fe} \cdot R_1 \| R_2}{r_{in} \quad R_1 \| R_2}$$

5. Power Gain

$$A_p = A_v \times A_i$$

Common Collector h-parameter Analysis

The CC transistor circuit and its h-parameter equivalent are shown in Fig.14

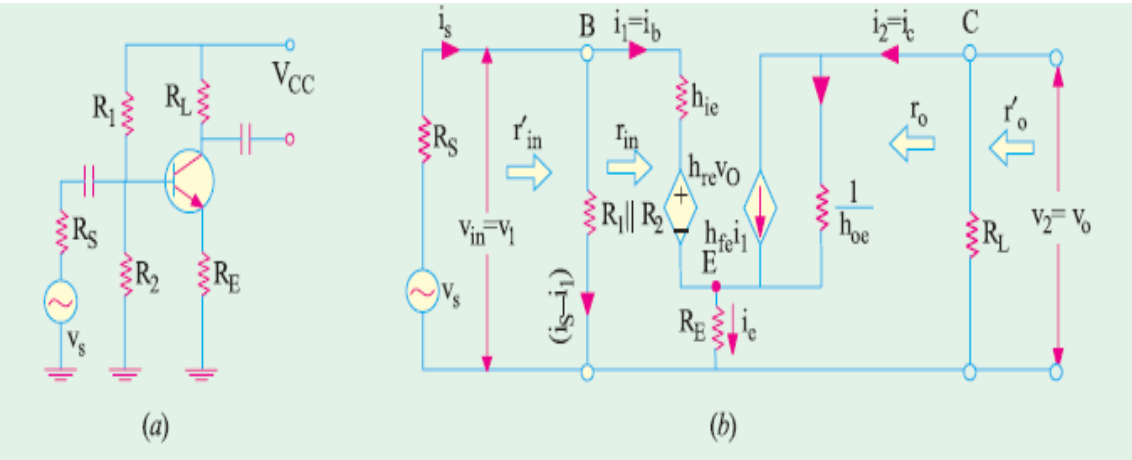


Fig.14

l. Input Impedance

$$v_{in} = i_b h_{ic} + h_{rc} v_o = i_b h_{ic} + v_o = i_b h_{ic} + i_e R_L$$
$$= i_b h_{ic} + h_{fe} i_b R_L = i_b (h_{ic} + h_{fe} R_L) \qquad i_c = h_{fe} i_b$$

$$\therefore \qquad r_{in} \quad \frac{v_{in}}{i_b} \quad h_{ic} \quad h_{fe} R_L$$

As seen, $r_{in(stage)} = r_{in(base)} \| R_1 \| R_2 = r_{in(base)} \| R_B$ where $R_B = R_1 \| R_2$

2. Output Impedance

$$r_o \quad \frac{v_2}{i_2}\Big|_{v_s\ 0} \qquad \frac{v_o}{i_c}\Big|_{v_s\ 0}$$

Now, $i_e \cong i_c = h_{fe} i_b = h_{fc} i_1$

Since $v_s = 0$, i_b is produced by $h_{rc} v_o = v_o$

Hence, considering the input circuit loop, we get

$$i_b \quad \frac{v_0}{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)} \quad \frac{v_0}{h_{ic} \quad R_S \parallel R_B}$$

$$i_c \quad h_{fc} i_b \quad \frac{h_{fc} v_o}{h_{ic} \quad (R_S \parallel R_B)} \qquad \text{where } R_B = R_1 \parallel R_2$$

$$\therefore \qquad r_o \quad \frac{V_o}{i_e} \quad \frac{h_{ic} \quad (R_S \parallel R_1 \parallel R_2)}{h_{fe}}$$

Also, r_o' or $r_{o(stage)} = r_o \parallel R_L$

3. Voltage Gain

$$A_v \quad \frac{v_2}{v_1} \quad \frac{v_o}{v_{in}}$$

Now, $v_o = i_e R_L = h_{fe} i_b R_L$ and $i_b = (v_{in} - v_o) / h_{ic}$

$$v_o \quad \frac{h_{fe} R_L}{h_{ie}} (v_{in} \quad v_o) \quad \text{or} \quad v_o \ 1 \quad \frac{h_{fe} R_L}{h_{ic}} \quad \frac{h_{fe} R_L v_{in}}{h_{ic}}$$

$$\therefore \qquad A_v \quad \frac{v_o}{v_{in}} \quad \frac{h_{fe} R_L / h_{ic}}{1 \quad h_{fe} R_L / h_{ic}} \quad 1$$

4. Current Gain

$$A_i \quad \frac{i_2}{i_1} \quad \frac{i_e}{i_b} \quad h_{fe}\ ; \ A_{is} \quad \frac{h_{fe} R_B}{r_{in} \quad R_B} \qquad \text{where } R_B = R_1 \parallel R_2$$

Conversion of h-parameters

Transistor data sheets generally specify the transistor in terms of its h-parameters for CB connection i.e. h_{ib}, h_{fb}, h_{rb} and h_{ob}. If we want to use the transistor in CE or CC configuration we will have to convert the given set of parameters into a set of CE or CC parameters. Approximate conversion formulae are tabulated over leaf :

Table

From CB to CE	*From CE to CB*	*From CE to CC*
$h_{ie} \quad \frac{h_{ib}}{1 \quad h_{fb}}$	$h_{ie} \quad \frac{h_{ie}}{1 \quad h_{fe}}$	$h_{ic} = h_{ic}$
$h_{oe} \quad \frac{h_{ob}}{1 \quad h_{fb}}$	$h_{ob} \quad \frac{h_{oe}}{1 \quad h_{fe}}$	$h_{oc} = h_{oe}$
$h_{fe} \quad \frac{h_{fb}}{1 \quad h_{fb}}$	$h_{fb} \quad \frac{h_{fe}}{1 \quad h_{fe}}$	$h_{fe} = -(1 + h_{fe})$
$h_{re} \quad \frac{h_{ib} h_{ob}}{1 \quad h_{fb}} \quad h_{rb}$	$h_{rb} \quad \frac{h_{ie} h_{oe}}{1 \quad h_{fe}} \quad h_{re}$	$h_{re} = 1 - h_{re} \cong 1$

Example. *A transistor used in CB circuit has the following set of parameters.*

$h_{ib} = 36\ \Omega, h_{fb} = 0.98, h_{rb} = 5 \times 10^{-4}, h_{ob} = 10^{-6}$ *Siemens*

With $R_S = 2$ *K and* $R_C = 10$ *K, calculate* (*i*) $r_{in(base)}$ (*ii*) r_{out} (*iii*) A_i and (*iv*) A_v.

Solution. Approximate Values

(*i*) $r_{in} = h_{ib} = 36\ \Omega$ (*ii*) $r_o \quad \frac{1}{h_{ob}} \quad \frac{1}{10^{-6}} \quad 1\text{M}$

(*iii*) $A_i = h_{fb} = -0.98$ (*iv*) $A_v \quad \frac{h_{fb}}{h_{ib}} \quad R_C \quad \frac{0.98}{36} \quad 10\text{K} \quad 272$

More Accurate Values

(*i*) $r_{in(base)} \quad h_{ib} \quad \frac{h_{rb} h_{fb}}{h_{ob} \quad 1/r_L}$

$= 36 \quad \frac{0.98 \quad 5 \quad 10^{-4}}{10^{-6} \quad 1/10 \quad 10^3}$ ($\therefore \quad r_L = R_C$ since there is no R_L)

$= 36 + 4.9 = 40.9\ \Omega$

It is the input resistance at transistor terminals.

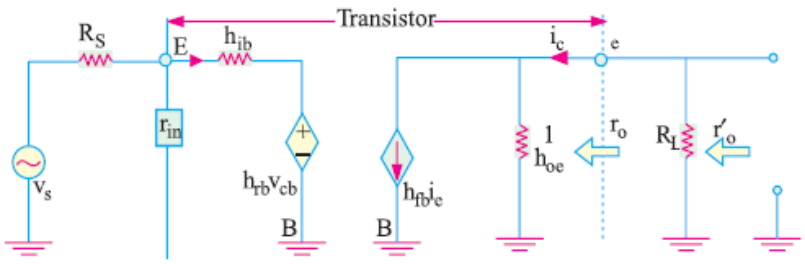


Fig. 15

(*ii*) $r_o \quad \frac{h_{ib} \quad R_s}{h_o (h_{ib} \quad R_S) \quad h_{fb} . h_{rb}} \quad \frac{36 \quad 2000}{10^{-6} (36 \quad 2000) \quad (0.98) \quad 5 \quad 10^{-4}} \quad 0.8\ \text{M}$

It is the output resistance at transistor terminals.

(*iii*) $A_i \quad \frac{h_{fb}}{1 \quad h_{ob} r_L} \quad \frac{0.98}{1 \quad 10^{-6} \quad 10^4} \quad -0.97$

(*iv*) $A_v \quad \frac{h_{fb} r_L}{h_{ib} (1 \quad h_{ob} r_L) \quad h_{fb} h_{rb} . r_L}$ ($r_L \quad R_L$)

Here, ac load $r_L = R_L = 10\ \text{K} = 104\ \Omega$

$\therefore \quad A_v \quad \frac{(0.98) \quad 10^4}{36 (1 \quad 10^{-6} \quad 10^4) \quad (0.98) \quad 5 \quad 10^{-4} \quad 10^4} \quad 249$

Example *A transistor used in CE connection has the following set of h-parameters : $h_{ir} = 1$ K, $h_{fe} = 100$, $h_{re} = 5 \times 10^{-4}$ and $h_{oc} = 2 \times 10^{-5}$ S. With $R_S = 2$ K and $R_C = 5$ K, determine*

(i) r_{in} (ii) r_o (iii) A_i and (iv) A_v

Solution.

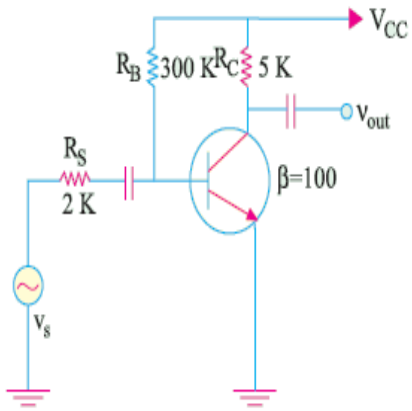


Fig. 16

(i) $r_{in} \quad h_{ie} \quad \dfrac{h_{fb} r_L}{h_o \quad 1/r_L}$

$= 1000 \quad \dfrac{5 \quad 10^{4} \quad 100}{2 \quad 10^{5} \quad 1/5 \quad 10^{3}}$

$= 723\ \Omega$

(ii) $r_o \quad \dfrac{h_{ie} \quad R_s}{(h_{ie} \quad R_s) h_{oe} \quad h_{fe} . h_{re}} \quad \dfrac{1000 \quad 2000}{(1000 \quad 2000) \quad 10^{5} \quad 100 \quad 5 \quad 10^{4}}$

$= 30{,}000\Omega = 0.03$ M

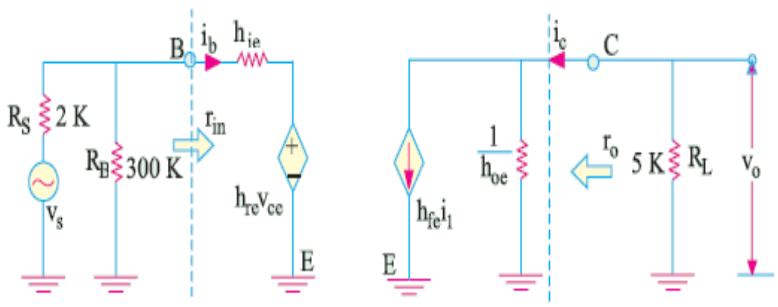


Fig. 17

(iii) $A_i \quad \dfrac{h_{fe}}{1 \quad h_{oe} r_L} \quad \dfrac{100}{1 \quad 2 \quad 10^{5} \quad 5 \quad 10^{3}} \quad 91$

(iv) $A_i \quad \dfrac{h_{fe} r_L}{(h_{ie} \quad R_s)(1 \quad h_{oe} . r_L) \quad h_{fe} h_{re} r_L}$

$$\frac{100 \quad 5 \quad 10^{3}}{(100 \quad 2000)(1 \quad 2 \quad 10^{5} \quad 5 \quad 10^{3}) \quad 100 \quad 5 \quad 10^{4} \quad 5 \quad 10^{3}} \quad -164$$

The negative sign indicates that there is 180° phase shift between the input and output ac signals. Obviously, it is the overall (or circuit) voltage gain and not the voltage gain of the transistor alone.

Example *The transistor of Fig. has the following set of h-parameters :*

$h_{ie} = 2\ \text{K}, h_{fe} = 100, h_{re} = 5 \times 10^{-4}, h_{oe} = 2.5 \times 10^{-5}\ \text{S}$

Find the voltage gain and the ac impedance of the stage.

Solution. Using somewhat exact formul

$$r_{in(base)} \quad h_{ie} \quad \frac{h_{fe}h_{re}}{h_{oe} \quad 1/r_L}$$

Now, collector load

$$r_L = 10\ \text{K} \parallel 30\ \text{K} = 7.5\ \text{K}$$

$$\therefore \quad r_{in(base)} \quad 200 \quad \frac{100 \quad 5 \quad 10^{4}}{2.5 \quad 10^{5} \quad 1/7.5 \quad 10^{3}}$$

$$= 2000 - 316 = \mathbf{1684\ \Omega}$$

The ac input impedance of the stage *i.e.* impedance when looking into point *B* is

$$r_{in(base)} = r_{in(base)} \parallel R_1 \parallel R_2 = 1.684 \parallel 50 \parallel 25 = \mathbf{1.53K}$$

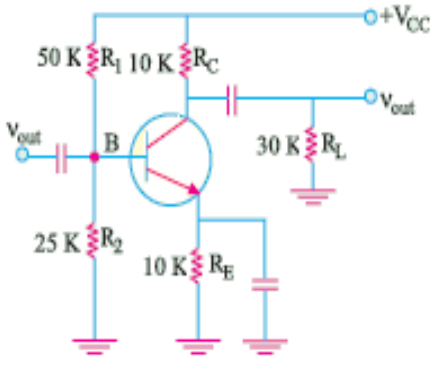


Fig.

$$A_v \quad \frac{h_{fe}}{r_{in(base)}(h_{oe} \quad 1/r_L)} \qquad \text{Now,} \quad r_L = 10\ \text{K} \parallel 30\ \text{K} = 7.5\ \text{K}$$

$$\therefore \quad A_v \quad \frac{100}{0184\ (2.5 \quad 10^{5} \quad 1/7500)} \quad \mathbf{-375}$$

Obviously, R_E does not come into the ac picture because it is ac grounded by the bypass capacitor.

Example *In the CC circuit of Fig. the transistor parameter are $h_{ie} = 2K$ and $h_{fe} = 100$. Calculate the circuit input and output impedance and voltage, current and power gains.*

Solution. $r_{in} \cong h_{ie} + h_{fe} R_L = 2 + 100 \times 5 = \mathbf{502\ K}$

$$r_{in(stage)} = R_1 \parallel R_2 \parallel r_{in}$$

$$= 10 \parallel 10 \parallel 502 = \mathbf{4.95\ K}$$

$$r_o \quad \frac{h_{ie} \quad (R_s \parallel R_1 \parallel R_2)}{h_{fe}}$$

$$\frac{2 \quad (1 \parallel 10 \parallel 100)}{100} \quad \mathbf{28.3\ \Omega}$$

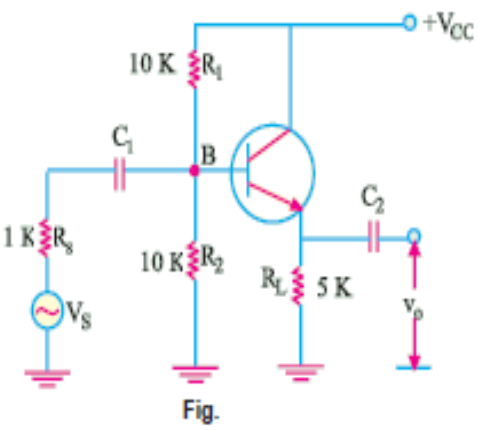


Fig.

$$r_{o(stage)} = r_o \parallel R_L = 28.3\ \Omega \parallel 5\text{K}$$

$$= \mathbf{28.1\Omega}$$

$$A_v \cong 1 \text{ and } A_i = h_{fe} = 100$$

1.What is an OP-AMP ?

It is a very high-gain, amplifier which can amplify signals having frequency ranging from **0 Hz to a little beyond 1 MHz.** They are made with different internal configurations in linear *ICs*. An *OP-AMP* is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation and integration etc. in analog computers. Present day usage is much wider in scope but the popular name *OP-AMP* continues.

Although an *OP-AMP* is a complete amplifier, it is so designed that external components (resistors, capacitors etc.) can be connected to its terminals to change its external characteristics. Hence, it is relatively easy to tailor this amplifier to fit a particular application and it is, in fact, due to this versatility that *OP-AMPs* have become so popular in industry.

2. OP-AMP Symbol

Standard triangular symbol for an *OP-AMP* is shown in Fig.1 (*a*) though the one shown in Fig.1 (*b*) is also used often. In Fig.1 (*b*), **the common ground line has been omitted.** It also does not show other necessary connections such as for dc power and feedback etc. The *OP-AMP's* input can be single ended or double-ended (or differential input) depending on whether input voltage is applied to one input terminal only or to both. Similarly, amplifier's output can also be either single-ended or double ended.

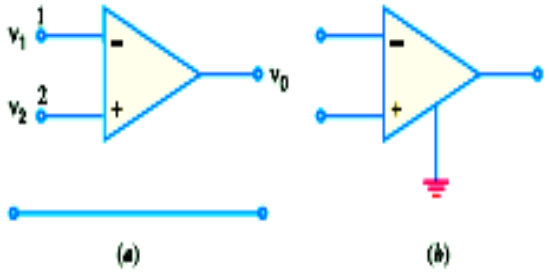
The most common configuration is ***two input terminals and a single output.***

All OP-AMPs have a minimum of five terminals :

1. inverting input terminal, **2.** non-inverting input terminal,

3. output terminal, **4.** positive bias supply terminal,

5. negative bias supply terminal.



3. OP-AMP Applications

We will consider the following applications :

1. As scalar or linear (*i.e.*, small-signal) constant-gain amplifier both inverting and non-inverting, **2.** as unity follower, **3.** Adder or Summer, **4.** Sub-tractor,

5. Integrator, **6.** Differentiator **7.** Comparator.

Now, we will discuss the above circuits one by one assuming an ideal *OPAMP*.

4. Linear Amplifier

We will consider the functioning of an *OP-AMP* as constant-gain amplifier both in the inverting and non-inverting configurations.

(*a*) Inverting Amplifier or Negative Scale.

As shown in Fig.2, non-inverting terminal has been grounded, whereas R_1 connects the input signal v_1 to the inverting input. A feedback resistor R_f has been connected from the output to the inverting input.

Gain

Since point A is at ground potential*, $i_1 = \frac{v_{in}}{R_1} = \frac{v_1}{R_1}$

$$i_2 = \frac{-v_0}{R_f} \quad \text{Please note –ve sign}$$

Using KCL

$$i_1 + (-i_2) = 0 \quad \text{or} \quad \frac{v_1}{R_1} + \frac{v_0}{R_f} = 0 \quad \text{or} \quad \frac{v_0}{R_f} = -\frac{v_1}{R_1} \quad \text{or} \quad \frac{v_0}{v_1} = -\frac{R_f}{R_1}$$

$$\therefore \quad A_v = -\frac{R_f}{R_1} \quad \text{or} \quad A_v = -K \quad \text{Also, } v_0 = -Kv_{in}$$

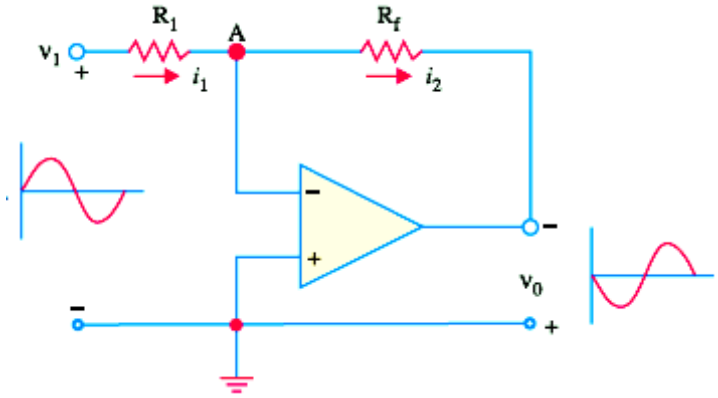


Fig.2

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors R_1 and R_f and is independent of the amplifier parameters. It is also seen that the *OP-AMP* works as a negative scaler. It scales the input *i.e.*, it multiplies the input by a minus constant factor K.

(*b*) Non-inverting Amplifier or Positive Scaler

This circuit is used when there is need for an output which is equal to the input multiplied by a positive constant. Such a positive scaler circuit which uses negative feedback but provides an output that equals the input multiplied by a positive constant is shown in Fig.3. Since input voltage v_2 is applied to the non-inverting terminal, the circuits is also called **non-inverting amplifier.**

Here, polarity of v_0 is the same as that v_2 *i.e.*, both are positive.

Gain

Because of virtual short between the two *OP-AMP* terminals, voltage across R_1 is the input voltage v_2. Also, v_0 is applied across the series combination of R_1 and R_f.

$$\therefore \quad v_{in} = v_2 = iR_1, v_0 = i(R_1 + R_f)$$

$$\therefore \quad A_v = \frac{v_0}{v_{in}} = \frac{i(R_1 + R_f)}{iR_1} \quad \text{or} \quad A_v = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

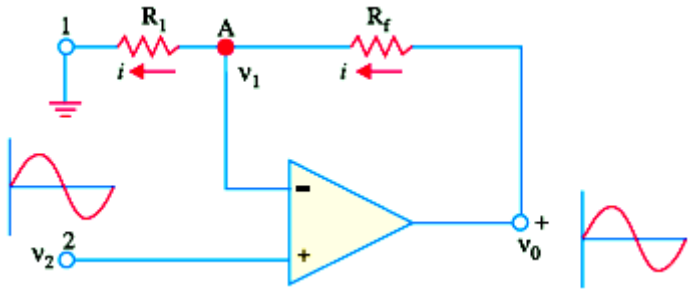


Fig.3

Example 68.1. *For the inverting amplifier of Fig. 68.5, R_1 = 1 K and R_f = 1 M. Assuming an ideal OP-AMP amplifier, determine the following circuit values :*

(a) voltage gain, (b) input resistance, (c) output resistance

Solution. It should be noted that we will be calculating values of the circuit and not *for* the *OP-AMP proper*.

(a) $$A_v = -\frac{R_f}{R_1} = -\frac{1000\ K}{1\ K} = -1000$$

(b) Because of virtual ground at A, $R_{in} = R_1 = 1\ K$

(c) Output resistance of the circuit equal the output resistance of the *OP-AMP i.e.*, zero ohm.

5. Unity Follower

It provides a gain of unity without any phase reversal. This circuit (Fig. 4) is useful as a buffer or isolation amplifier because it allows, input voltage v_{in} to be transferred as output voltage v_0 while at the same time preventing load resistance

R_L from loading down the input source. It is due to the fact that its $R_i = \infty$ and $R_0 = 0$. In fact, circuit of Fig. 4 can be obtained from that of Fig. 2 by putting

$$R_1 = R_f = 0.$$

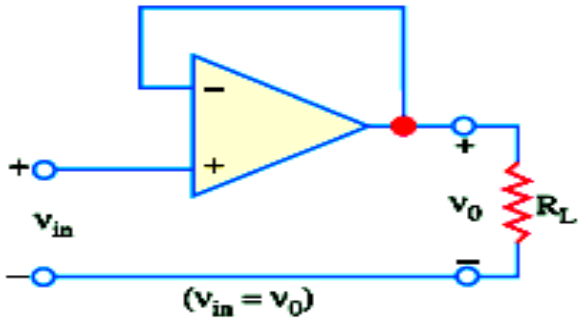


Fig.4

6. Adder to Summer

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. Fig. 5 shows a three-input inverting adder circuit. As seen, *the* ***output voltage is phase-inverted.***

Calculations

As before, we will treat point *A* as virtual ground

$$i_1 = \frac{v_1}{R_1} \quad \text{and} \quad i_2 = \frac{v_2}{R_2}$$

$$i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_0}{R_f}$$

Applying *KCI* to point *A*, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or
$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_0}{R_f}\right) = 0$$

$\therefore$
$$v_0 = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right)$$

or
$$v_0 = -(K_1 v_1 + K_2 v_2 + K_3 v_3)$$

The overall negative sign is unavoidable because we are using the inverting input terminal.

If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R}(v_1 + v_2 + v_3) = -K(v_1 + v_2 + v_3)$$

Hence, output voltage is proportional to **(*not equal to*)** the **algebraic sum** of the three input voltages.

If $R_f = R$, then ouput exactly equals the sum of inputs. However, if $R_f = R/3$

then $$v_0 = -\frac{R/3}{R}(v_1 + v_2 + v_3) = -\frac{1}{3}(v_1 + v_2 + v_3)$$

7. Subtractor

The function of a subtractor is to provide an output proportional to or equal to the difference of two input signals. As shown in Fig. 6 we have to apply the inputs at the inverting as well as noninverting terminals.

Calculations

According to Superposition Theorem $v_0 = v_0' + v_0''$ where v_0' is the output produced by v_1 and v_0'' is that produced by v_2.

Now, $\quad v_0' = -\dfrac{R_f}{R_1} \cdot v_1$

$$v_0'' = \left(1 + \frac{R_f}{R_1}\right) v_2$$

$$\therefore \quad v_0 = \left(1 + \frac{R_f}{R_1}\right) v_2 - \frac{R_f}{R_1} \cdot v_1$$

Since $R_f \gg R_1$ and $R_f/R_1 \gg 1$, hence

$$v_0 \equiv \frac{R_f}{R_1}(v_2 - v_1) = K(v_2 - v_1)$$

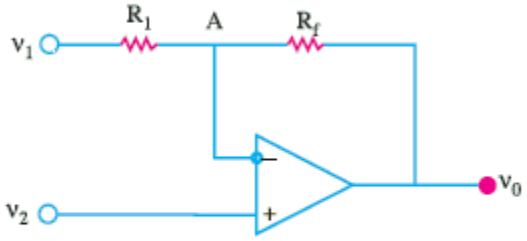


Fig. 6

Further, If $R_f = R_1$, then

$$v_0 = (v_2 - v_1) = \text{difference of the two input voltages}$$

Obviously, if $R_f \neq R_1$, then a scale factor is introduced.

Example *Find the output voltages of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, $R_f = 1\ M$.*

$$v_1 = -3\ V, v_2 = +3V, v_3 = +2V; R_1 = 250\ K, R_2 = 500\ K, R_3 = 1\ M$$

Solution. $\quad v_0 = -(K_1 v_1 + K_2 v_2 + K_3 v_3)$

$$K_1 = \frac{R_f}{R_1} = \frac{1000\ K}{250\ K} = 4, K_2 = \frac{1000}{500} = 2, K_3 = \frac{1M}{1M} = 1$$

$$\therefore \quad v_0 = -[(4 \times -3) + (2 \times 3) + (1 \times 2)] = +\mathbf{4V}$$

Example *Design an OP-AMP circuit that will produce an output equal to* $-(4\ v_1 + v_2 + 0{\cdot}1\ v_3)$. *Write an expression for the output and sketch its output waveform when* $v_1 = 2 \sin \omega t$, $v_2 = +5$ *V dc and* $v_3 = -100$ *V dc.*

Solution.

$$v_0 = -\left[\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3\right] \quad \ldots(1)$$

and also

$$v_0 = -(4\ v_1 + v_2 + 0{\cdot}1\ v_3) \quad \ldots(2)$$

Comparing equations (1) and (2), we find,

$$\frac{R_f}{R_1} = 4,\ \frac{R_f}{R_2} = 1,\ \frac{R_f}{R_3} = 0{\cdot}1$$

Therefore if we assume $R_f = 100\ K$, then $R_1 = 25\ K$, $R_2 = 100\ K$ and $R_3 = 10\ K$. With there values of R_1, R_2 and R_3, the *OP-AMP* circuit is as shown in Fig.

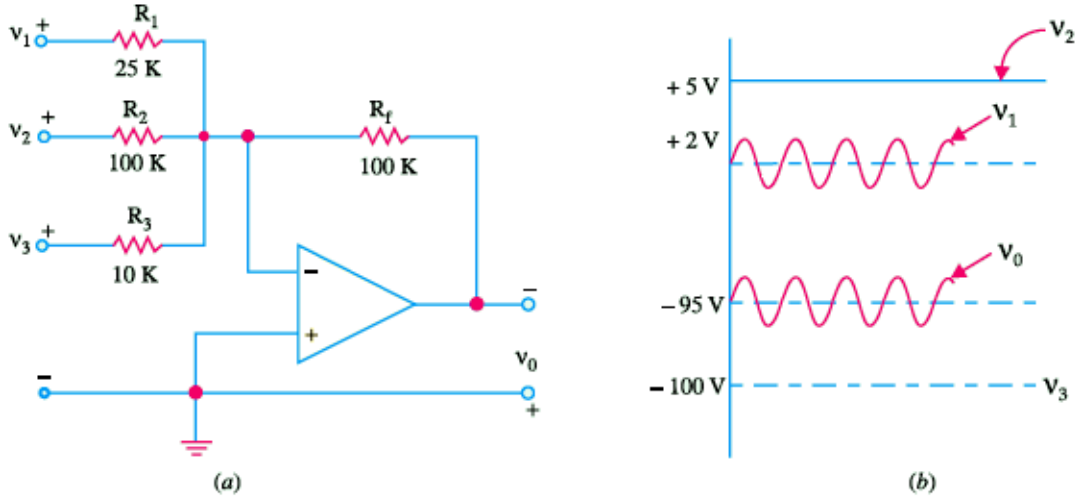
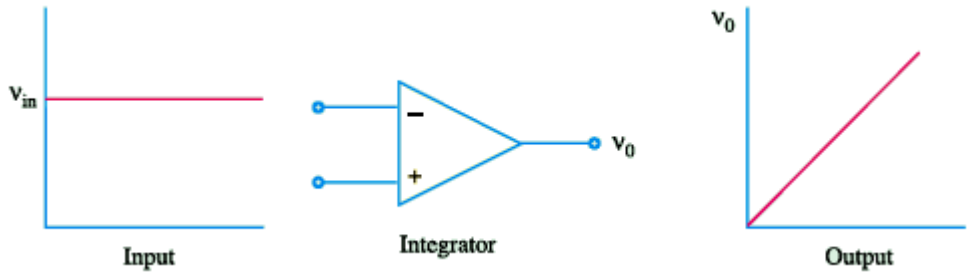


Fig.

With the given values of $v_1 = 2 \sin \omega t$, $v_2 = +5$V, $v_3 = -100$ V dc, the output voltage, $v_0 = 2 \sin \omega t + 5 - 100 = 2 \sin \omega t - 95$ V. The waveform of the output voltage is sketched as shown in Fig. (*b*).

8. Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage.



A simple example of integration is shown in Fig. 7 where input is dc level and its integral is ***a linearly-increasing ramp output.*** This circuit is that **the feedback component is a capacitor C instead of a resistor R_f.**

Calculations

As before, point *A* will be treated as virtual ground.

$$i_1 = \frac{v_1}{R}\ ;\ i_2 = -\frac{v_0}{X_C} = -\frac{v_0}{1/j\omega C} = -\frac{v_0}{1/sC} = -s\,C\,v_0$$

where $s = j\,\omega$ in the Laplace notation.

Now $i_1 = i_2$ ...Art. 68.26 (*a*)

$$\therefore \quad \frac{v_1}{R} = -s\,Cv_0$$

$$\therefore \quad \frac{v_0}{v_{in}} = \frac{v_0}{v_1} = -\frac{1}{s\,CR} \qquad ...(i)$$

$$\therefore \quad A_v = -\frac{1}{s\,CR}$$

Now, the expression of Eq. (*i*) can be written in time domain as

$$v_0(t) = -\frac{1}{40\,\pi}(\cos 2000\,\pi t - 1)$$

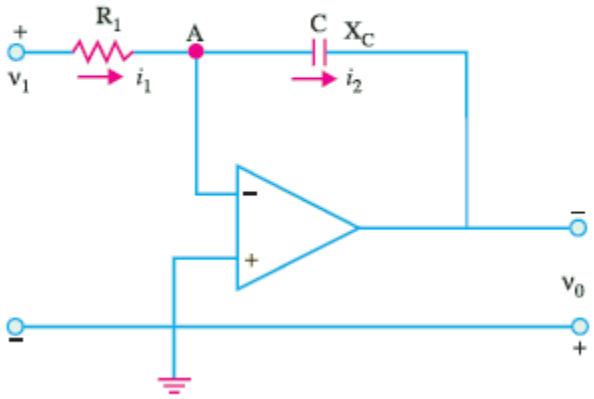


fig.7

It is seen from above that output (right-hand side expression) is an integral of the input, with an inversion and a scale factor of 1/*CR*. This ability to integrate a given signal enables an analog computer solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operation. For example, let *R* = 1 M and *C* = 1 μF. Then

$$\textbf{scale factor} = -\frac{1}{CR} = -\frac{1}{10^6 \times 10^{-6}} = -1$$

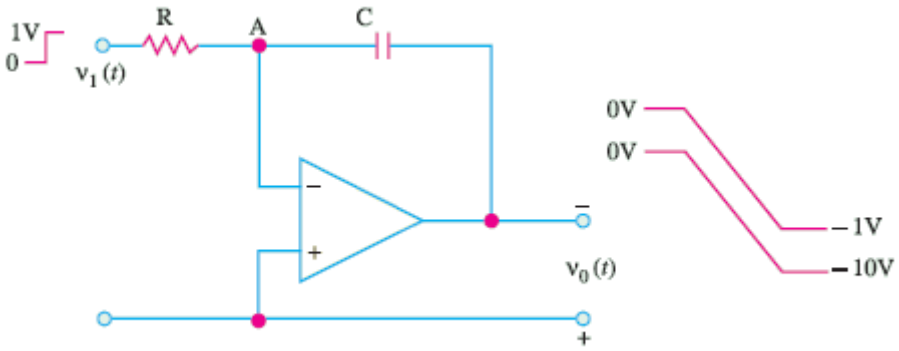


Fig.8

As shown in Fig. 8 the input is a step voltage, whereas output is a ramp (or linearly-changing voltages) with a scale multiplier of −1. However, when R = 100 K, then

$$\text{scale factor} = -\frac{1}{10^5 \times 10^{-6}} = -10$$

$$\therefore \quad v_0(t) = -10 \int v_1(t) \, . \, dt$$

9. Differentiator

Its function is to provide an output voltage which is ***proportional to the rate of the change of the input voltage*.** It is an inverse mathematical operation to that of an integrator. As shown in Fig. 9, when we feed a differentiator with linearly-increasing ramp input, we get a constant dc output.

Circuit

Differentiator circuit can be obtained by interchanging the resistor and capacitor of the integrator circuit of Fig. 8. Let i = rate of change of charge $=dq/dt$.

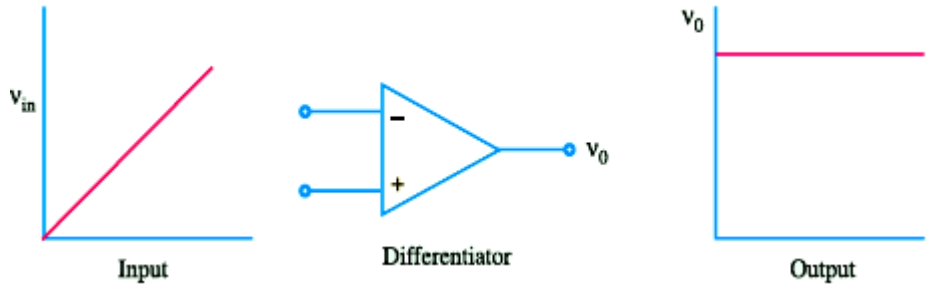


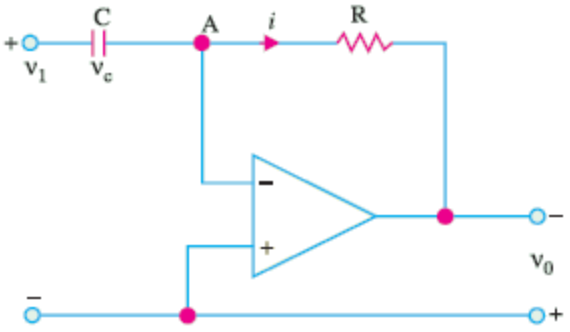
Fig.9

Now, $q = Cv_c$

$$\therefore \quad i = \frac{d}{dt}(Cv_c) = C\frac{dv_c}{dt}$$

Taking point A as virtual ground

$$v_0 = -iR = -\left(C \cdot \frac{dv_c}{dt}\right)R = -CR \cdot \frac{dv_c}{dt}$$



Example *The input to the differentiator cir cuit of Fig. is a sinusoidal voltage of peak value of 5 mV and frequency 1 kHz. Find out the output if R = 1000 K and C = 1 μF.*

Solution. The equation of the input voltage is

$$v_1 = 5 \sin 2\pi \times 1000\, t = 5 \sin 2000\, \pi t \text{ mV}$$

scale factor $= CR = 10^{-6} \times 10^{5} = 0{\cdot}1$

$$v_0 = 0{\cdot}1 \frac{d}{dt}(5 \sin 2000\, \pi t) = (0{\cdot}5 \times 2000\, \pi) \cos$$

$2000\, \pi t = 1000\, \pi \cos 2000\, \pi t$ mV

As seen, output is a cosinusoidal voltage of frequency 1 kHz and peak value 1000 π mV.

10. Comparator

It is a circuit which compares two signals or voltage levels. The circuit is shown in Fig. 10 and (like that of the unity follower) is the simplest because it needs no additional external components.

If v_1 and v_2 are equal, then v_0 should ideally be zero. Even if v_1 differs from v_2 by a very small amount, v_0 is large because of amplifier's high gain. Hence, circuit of Fig.10 can detect very small changes which is another way of saying that it compares two signals.

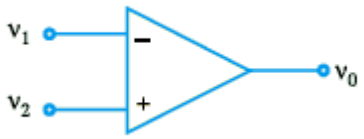


Fig.10

1. What is a FET ?

The acronym 'FET' stands for **field effect transistor**. It is a three-terminal unipolar solid-state device in which current is controlled ***by an electric field*** as is done in vacuum tubes. Broadly speaking, there are two types of FETs :

(*a*) junction field effect transistor (JFET)

(*b*) metal-oxide semiconductor FET (MOSFET)

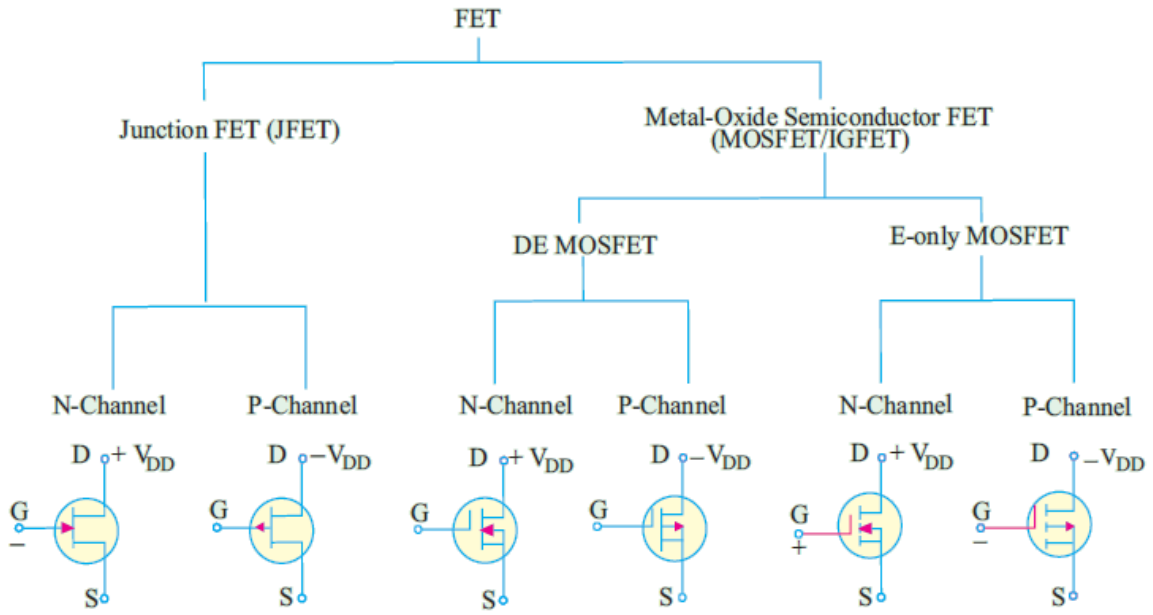
It is also called insulated-gate FET (IGFET). It may be further subdivided into :

(*i*) depletion-enhancement MOSFET *i.e.* DEMOSFET

(*ii*) enhancement-only MOSFET *i.e.* E-only MOSFET

Both of these can be either *P*-channel or *N*-channel devices.

The FET family tree is shown below :



Advantages of FETs

FETs combine the many advantages of both BJTs and vacuum tubes. Some of their main advantages are :

1. high input impedance, **2.** small size, **3.** ruggedness, **4.** long life,

5. high frequency response, **6.** low noise,

7. negative temperature coefficient, hence better thermal stability,

8. high power gain,

9. a high immunity to radiations,

10. no offset voltage when used as a switch (or chopper), **11.** square law characteristics.

The only disadvantages are :

1. small gain-bandwidth product,

2. greater susceptibility to damage in handling them.

2. Static Characteristics of a JFET

We will consider the following two characteristics:

(*i*) drain characteristic

It gives relation between I_D and V_{DS} for different values of V_{GS} (which is called running variable).

(*ii*) transfer characteristic

It gives relation between I_D and V_{GS} for different values of V_{DS}.

We will analyse these characteristics for an *N*-channel JFET connected in the common-source mode as shown in Fig. 1. We will first consider the drain characteristic when $V_{GS} = 0$ and then when V_{GS} has any negative value up to $V_{GS(off)}$.

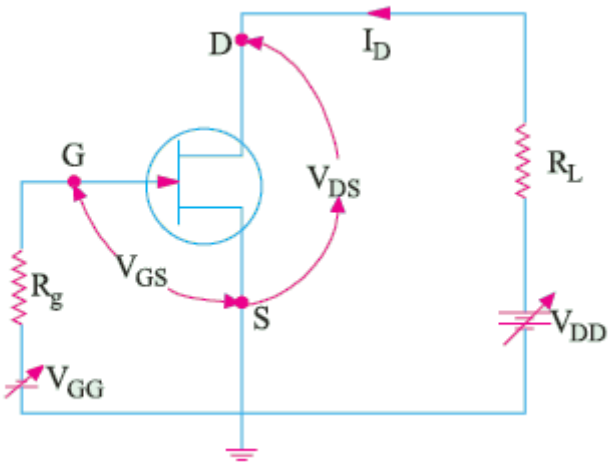


Fig.1

D.C Analysis of FET circuit

1. JFET C/CS:

a. output c/cs or Drain c/cs:

Fig. 2 shows a family of I_D versus V_{DS} curves for different values of V_{GS}. It is seen that as the negative gate bias voltage is increased**.** The *P-N* junctions must be reverse-biased for active region operation V_{GS}=-1V.

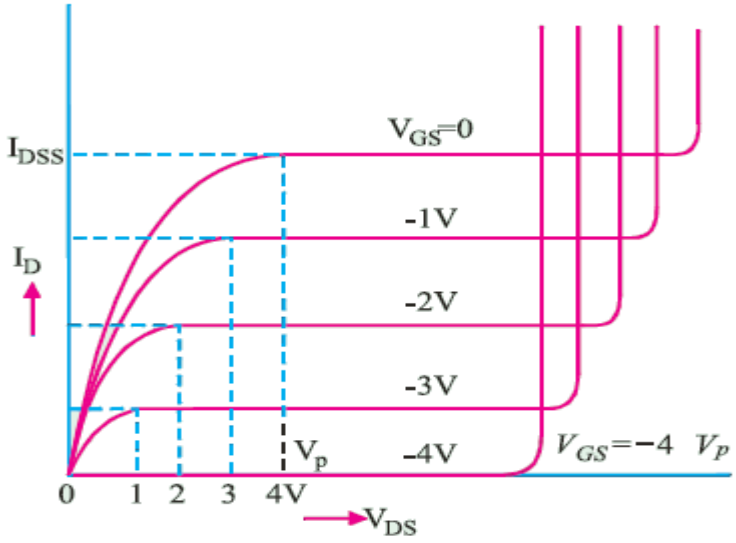


Fig.2

b. Transfer Characteristic

It is a plot of I_D versus V_{GS} for a constant value of V_{DS} and is shown in Fig. 3. It is similar to the transconductance characteristics of a vacuum tube or a transistor. It is seen that when V_{GS} = 0, I_D =I_{DSS} and when I_D = 0, V_{GS} = V_P. The transfer characteristic approximately follows the equation.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

The above equation can be written as

$$V_{GS} = V_{GS(off)}\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right)$$

This characteristic can be obtained from the drain characteristics by reading off V_{GS} and I_{DSS} values for different values of V_{DS}.

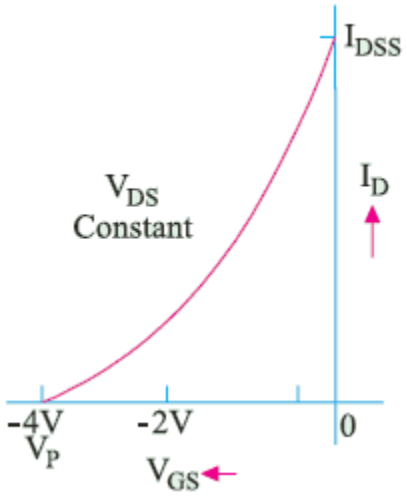


Fig.3

3. DC Biasing of a JFET

A JFET may be biased by using either

1. A separate power source V_{GG} as shown in Fig. 4 (*a*),

2. Some form of self-bias as shown in Fig. 4(*b*),

3. Source bias as in Fig. 4 (*c*),

4. Voltage divider bias as in Fig. 4 (*d*).

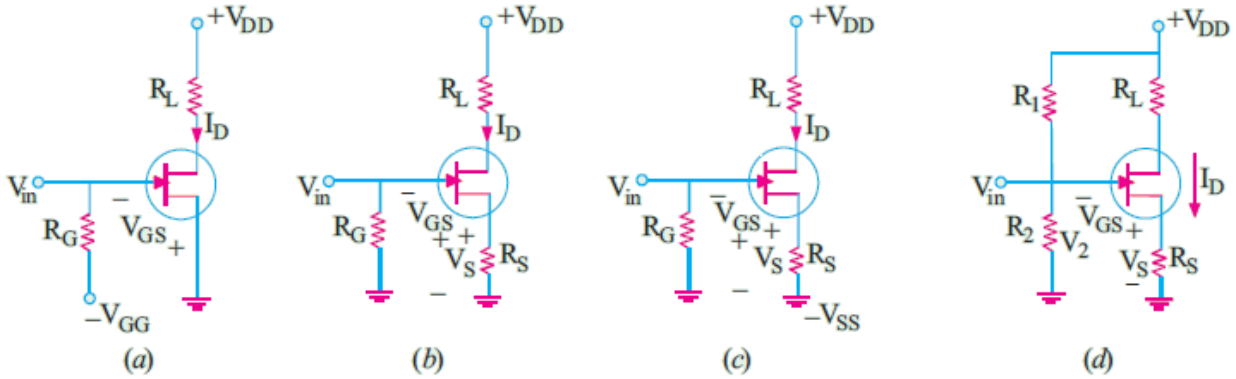


Fig.4

$V_{GS}=V_{GG}$

Given I_{DSS}, V_P

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1-\frac{V_{GS}}{V_{GS(off)}}\right)^2$$

$I_G=0$, $I_D=I_S$

$V_D=V_{DD}-I_D R_D$

$V_S=0$

$V_{DS}=V_D-V_S=V_{DD}-I_D R_D$

$P_D=I_D V_{DS}$.

The circuit of Fig. 4 (*b*) is called self-bias circuit because the V_{GS} bias is obtained from the flow of JFET's own drawn current I_D through R_S.

$\therefore V_S = I_D R_S$ and $V_{GS} = - I_D R_S$

The gate is kept at this much negative potential with respect to the ground.

The addition of R_G in Fig. 4 (*b*), does not upset this dc bias for the simple reason that no gate current flows through it (the gate leakage current is almost zero). Hence, gate is essentially at ***dc ground*.** Without R_G, gate would be kept 'floating' which could collect charge and ultimately cutoff the JFET.

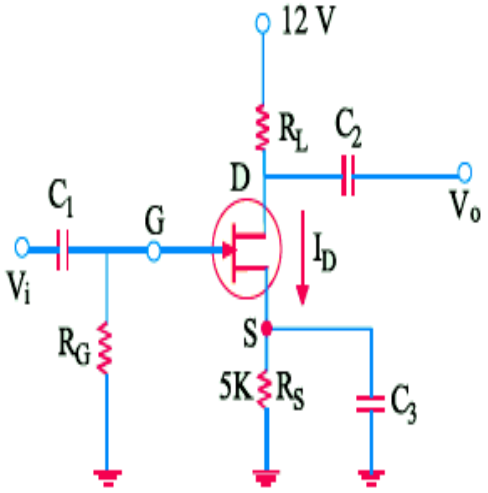
The resistance R_G additionally serves the purpose of avoiding short-circuiting of the ac input voltage, v_{in}. Moreover, in case leakage current is not totally negligible, R_G would provide it an escape route. Otherwise, the leakage current would build up static charge (voltage) at the gate which could change the bias or even destroy the JFET. Fig. 4 (*c*) shows the *source* bias circuit which employs a self-bias resistor R_S to obtain V_{GS}.

Here, $V_{SS} = I_D R_S + V_{GS}$ or $V_{GS} = V_{SS} - I_D R_S$.

Fig. 4(*d*) shows the familiar voltage divider bias. In this case, $V_2 = V_{GS} + I_D R_S$ or $V_{GS} = V_2 - I_D R_S$

$$\text{Since,} \quad V_2 = V_{DD} \frac{R_2}{R_1 + R_2} \qquad \therefore V_{GS} = V_{DD} \frac{R_2}{R_1 + R_2} - I_D R_S$$

Example *Determine the quiescent value of V_{GS} I_D and V_{DS} for the JFET circuit of Fig. given that $I_{DSS} = 10$ mA, $R_S = 5$ K and $V_P = -5$ V.*



Solution. Since $I_S \cong I_D$, $V_{GS} = -I_D R_S = -5000\, I_D$

Now, $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10 \times 10^{-3}\left(1 - \frac{V_{GS}}{-5}\right)^2$$

$$= 10 \times 10^{-3}(1 + 0.2\, V_{GS})^2$$

Substituting this value in the above equation, we get

$$V_{GS} = -5000(10 \times 10^{-3})(1 + 0.2\, V_{GS})$$

Expanding and rearranging the above, we have

$$2V_{GS}^2 + 21V_{GS} + 50 = 0$$

$$\therefore \quad V_{GS} = -3.65 \text{ V} \quad \text{or} \quad -6.85 \text{ V}$$

Rejecting the higher value because it is more than V_P, we have $V_{GS} = -3.65$ V

$$\therefore \quad -3.65 = -5000\, I_D \quad \therefore \quad I_D = 0.73 \text{ mA}$$

$$V_D = V_{DD} - I_D R_L = 12 - 0.73 \times 2 = 1.54 \text{ V}$$

$$V_S = I_D R_S = 0.73 \times 5 = 3.65\ V \quad \therefore \quad V_{DS} = V_D - V_S = 10.54 - 3.65 = 6.89 \text{ V}$$

1. Number Systems

The number systems are used quite frequently in the field of digital electronics and computers. However the type of number system used in computers could be different at different stages of the usage. For example, when a user key-in some data into the computer, s(he), will do it using decimal number system *i.e.* the system we all have used for several years for doing arithmetic problems. But when the information goes inside the computer, it needs to be converted to a form suitable for processing data by the digital circuitry. Similarly when the data has to be displayed on the monitor for the user, it has to be again in the decimal number system. Hence the conversion from one number system to another one is an important topic to be understood.

There are four systems of arithmetic which are often used in digital circuits. These systems are:

1. Decimal—it has a base (or radix) of 10 *i.e.* it uses 10 different symbols to represent numbers.

2. Binary—it has a base of 2 *i.e.* it uses only two different symbols.

3. Octal—it has a base of 8 *i.e.* it uses eight different symbols.

4. Hexadecimal—it has a base of 16 *i.e.* it uses sixteen different symbols.

All these systems use the same type of **positional notation** except that — decimal system uses powers of 10 — binary system uses power of 2 — octal system uses powers of 8 — hexadecimal system uses powers of 16.

Decimal numbers are used to represent quantities which are outside the digital system. Binary system is extensively used by digital systems like digital computers which operate on binary information. Octal system has certain advantages in digital work because it requires less circuitry to get information into and out of a digital system. Moreover, it is easier to read record and print out octal numbers

than binary numbers. Hexadecimal number system is particularly suited for microcomputers.

2. Binary Number System

Like decimal number (or denary) system, it has a radix and it also uses the same type of position value system.

(*i*) Radix

Its base or radix is **two** because it uses only two digits 0 and 1 (the word 'binary digit' is contracted to **bit**). All binary numbers consist of a string of 0s and 1s. Examples are 10, 101 and 1011 which are read as one zero, one-zero-one and one-zero-one one to avoid confusion with decimal numbers. Another way to avoid confusion is to add a subscript of 10 for decimal numbers and of 2 for binary numbers as illustrated below.

10_{10}, 101_{10}, 5742_{10} —decimal number and10_2, 101_2, 110001_2 — binary numbers.

It is seen that the subscript itself is in decimal. It may be noted that binary numbers need ***more places for counting because their base is small***

3. Binary to Decimal Conversion

Following procedure should be adopted for converting a given binary integer (whole number) into its equivalent decimal number:

Step 1. Write the binary number *i.e.* all its bits in a row.

Step 2. Directly under the bits, write 1, 2, 4, 8, 16,..... starting from *right to left*.

Step 3. Cross out the decimal weights which lie under 0 bits.

Step 4. Add the remaining weights to get the decimal equivalent.

Example. *Convert 11001_2 to its equivalent decimal number.*

Solution. The four steps involved in the conversion are as under

Step 1. 1 1 0 0 1

Step 2. 16 8 4 2 1

Step 3. 16 8 **4 2** 1

Step 4. 16 + 8 + 1 = 25 $\therefore 11001_2 = 25_{10}$

It is seen that the number contains 1 sixteen, one eight, 0 four's, 0 two's and 1 one.

4. Decimal to Binary Conversion

(*a*) Integers

Such conversion can be achieved by using the so-called **double-dabble method.** It is also known as **divide-by-two** method. In this method, we progressively divide the given decimal number by 2 and write down the remainders after each division. These remainders taken in the *reverse* order (*i.e.* from bottom-to-top) form the required binary number. As an example, let us convert 2510 into its binary equivalent.

25 ÷ 2 = 12 + remainder of 1

12 ÷ 2 = 6 + remainder of 0

6 ÷ 2 = 3 + remainder of 0

3 ÷ 2 = 1 + remainder of 1

1 ÷ 2 = 0 + remainder of 1

$25_{10} = 11001_2$

The above process may be simplified as under: ***Successive Remainders Divisions***

2) 25

2) 12 1

2) 6 0

2) 3 0

2) 1 1

2) 0 1

Reading the remainders from bottom to top, we get $25_{10} = 11001_2$. It may also be put in the following form:

25 ÷ 2 = 12 + 1

12 ÷ 2 = 6 + 0

6 ÷ 2 = 3 + 0

3 ÷ 2 = 1 + 1

1 ÷ 2 = 0 + 1

decimal 25 = 1 1 0 0 1 binary

5. Binary Operations

We will now consider the following four binary operations:

1. addition **2.** subtraction **3.** multiplication **4.** division

Addition is the most important of these four operations. In fact, by using **'complements'**, subtraction can be reduced to addition. Most digital computers subtract by complements. It leads to reduction in hardware because only adding type of circuits are required. Similarly, multiplication is nothing but repeated addition and, finally, division is nothing but repeated subtraction.

5.1 Binary Addition

Addition is simply the manipulation of numbers for combining physical quantities. For example, in the decimal number system, 2 + 3 = 5 means the combination of • • with • • • to give a total of • •• • •. Addition of binary numbers is similar to the decimal addition.

Following points will help in understanding the rules of binary addition.

1. When 'nothing' is combined with 'nothing', we get nothing. Binary representation of the above statement is: 0 + 0 = 0

2. When nothing is combined with •, we get •. In binary language 0 + 1 = 1

3. Combining • with nothing, gives •. The binary equivalent is 1 + 0 = 1

4. When we combine • with •, we get • •. The binary representation of the above is 1 + 1 = 1 0. It should be noted that the above sum is not 'ten' but 'one-zero' *i.e.* it represents • • and not • • • • • • • • • •. In other words, it is 10_2 which represents decimal 2. ***It is not decimal ten.*** The last rule is often written as 1 + 1 = 0 with a carry of 1

The above rules for binary addition can be summarized as under:

0 + 0 = 0 0 + 1 = 1

1 + 0 = 1 1 + 1 = 0 with a carry of 1 or $=10_2$

It is worth noting that 'carry-overs' are performed in the same manner as in decimal arithmetic. The rules of binary addition could also be expressed in the form of a table as shown below

		0	1			0	1
0	0	1		or	0	0	1
1	1	10_2			1	1	0

with a carry 1

As an illustration, let us add 101 and 110.

	1 0 1	— first column	1 + 0 = 1
+	1 1 0	— second column	0 + 1 = 1
	1 0 1 1	— third column	1 + 1 = 10

(*i.e.* 0 with carry 1)

Similarly,

	1 carry		
	1 1 1	— 1st column	1 + 0 = 1
+	1 1 0	— 2nd column	1 + 1 = 0 with carry 1
	1 1 0 1	— 3rd column	1 + 1 + carry of 1
			= 10 + 1 = 11_2

Let us consider one more example :

	1 carry	← 1 1 carry	← 1 1 carry	← 1 1 carry
	1 0 1 1	1 0 1 1	1 0 1 1	1 0 1 1
+	1 0 0 1	+ 1 0 0 1	+ 1 0 0 1	+ 1 0 0 1
	0	0 0	1 0 0	1 0 1 0 0

Hence, we find from the above examples that the only two possible combinations with a carry are :

(*a*) 1 + 1 = sum of 0 with a carry of 1. It is binary 10 *i.e.* 10_2 which equals *decimal* 2.

(*b*) 1 + 1 + carry of 1 = a sum of 1 with a carry of 1. It equals binary 11 *i.e.* 11_2 or decimal 3.

5.2 Binary Subtraction

It is also performed in a manner similar to that used in decimal subtraction. Because binary system has only two digits, binary subtraction requires more borrowing operations than decimal subtraction. The four rules for binary subtraction are as under:

1. 0 − 0 = 0, **2.** 1 − 0 = 1, **3.** 1 − 1 = 0, **4.** 0 − 1 = 1 with a borrow of 1 from the next column of the minuend or 10 − 1 = 1

The last result represents • • − • − • which makes sense.

While using Rule 4, it should be borne in mind that borrow reduces the remaining minuend by 1.

It means that a borrow will cause a 1 in the next column to the left in the minuend to become 0. If the next column also happens to contain 0, it is changed to a 1 and the succeeding 0s in the minuend are changed to 1s until a 1 is found which is then changed to a 0.

5.3 Binary Multiplication

The procedure for this multiplication is the same as for decimal multiplication though it is comparatively much easier. The four simple rules are as under:

1. $0 \times 0 = 0$, **2.** $0 \times 1 = 0$, **3.** $1 \times 0 = 0$, **4.** $1 \times 1 = 1$.

The rules of binary multiplication could be summarized in the form of a table as shown.

	0	1
0	0	0
1	0	1

As in the decimal system, the procedure is

1. copy the multiplicand when multiplier digit is 1 but not when it is 0

2. shift as in decimal multiplication

3. add the resulting binary numbers according to the rules of binary addition.

5.4 Binary Division

It is similar to the division in the decimal system. As in that system, here also division by 0 is meaningless. Rules are:

1. $0 \div 1 = 0$ or $\frac{0}{1} = 0$, **2.** $1 \div 1 = 1$ or $\frac{1}{1} = 1$.

6. Octal Number System

(*i*) Radix or Base

It has a base of 8 which means that it has eight distinct counting digits: 0, 1, 2, 3, 4, 5, 6, and 7. These digits 0 through 7, have exactly the same physical meaning as in decimal system. For counting beyond 7, **2-digit combinations are formed taking the second digit followed by the first, then the second followed by the second and so on.** Hence, after 7, the next octal number is 10 (second digit followed by first), then 11 (second digit followed by second) and so on. Hence, different octal numbers are :

0,	1,	2,	3,	4,	5,	6,	7,
10,	11,	12,	13,	14,	15,	16,	17,
20,	21,	22,	23,	24,	25,	26,	27,
30,	31,	32,	...	...	...	...	...

6.2 Binary to Octal Conversion

The simplest procedure is to use **binary-triplet** method. In this method, the given binary number is arranged into groups of 3 bits starting from the octal point and then each group is converted to its equivalent octal number. Of course, where necessary, extra 0s can be added **in front** (*i.e.* left end) of the binary number to complete groups of three. Suppose, we want to convert 101011_2 into its octal equivalent. Converting the bits into groups of three, we have

101 011

Now, 101_2 is 5 octal and 011 is 3 octal.

$\therefore$ 101 011

↓ ↓

5 3 $\therefore$ $101\ 011_2 = 53_8$

Now, take 111110111_2. We will first split it into groups of three bits (space is left between the groups for easy reading). Then, each group is given its octal number as shown below.

111 110 111

↓ ↓ ↓

7 6 7 $\therefore$ $111\ 110\ 111_2 = 767_8$

Table No. 69.3

Binary	*Octal*	*Binary*	*Octal*
000	0	1010	12
001	1	1011	13
010	2	1100	14
011	3	1101	15
100	4	1110	16
101	5	1111	17
110	6	10000	20
111	7	10001	21
1000	10	10010	22
1001	11	10011	23

7. Hexadecimal Number System

The characteristics of this system are as under:

1. it has a base of 16. Hence, it uses sixteen distinct counting digits 0 through 9 and A through F as detailed below :

0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F

2. place value (or weight) for each digit is in **ascending powers** of 16 for integers and **descending powers** of 16 for fractions.

The chief use of this system is in connection with **byte-organised machines.** It is used for specifying addresses of different binary numbers stored in computer memory.

7.1 Binary to Hexadecimal Conversion

The simple method is to split the given binary number into **4-bit groups** (supplying 0s from our own side if necessary) and then give each group its 'hex' value as found from Table.

Table No. 69.5

Binary	Hex.	Binary	Hex.	Binary	Hex.
0000	0	0110	6	1100	C
0001	1	0111	7	1101	D
0010	2	1000	8	1110	E
0011	3	1001	9	1111	F
0100	4	1010	A	10000	10
0101	5	1011	B	10001	11

Definition of a Logic Gate

A logic gate is an electronic circuit **which makes logic decisions**. It has one output and one or more inputs. The output signal appears only for certain combinations of input signals. Logic gates are the basic building blocks from which most of the digital systems are built up. They implement the hardware logic function based on the logical algebra developed by George Boole which is called Boolean algebra in his honour. A unique characteristic of the Boolean algebra is that variables used in it **can assume only one of the two values** *i.e.* either 0 or 1. Hence, every variable is either a 0 or a 1.

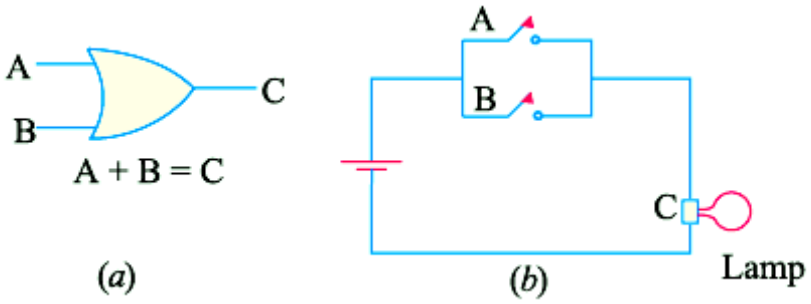
These gates are available today in the form of various IC families. The most popular families are: transistor-transistor logic (*TTL*), emitter-coupled logic (*ECL*), metal-oxide-semiconductor (*MOS*) and complementary metal-oxide-semiconductor (*CMOS*).

The OR Gate

The electronic symbol for a two-input *OR* gate is shown in Fig. 1 (*a*) and its equivalent switching circuit in Fig.1 (*b*). The two inputs have been marked as *A* and *B* and the output as *X*. It is worth reminding the reader that as per Boolean algebra, the three variables *A*, *B* and *X* can have only one of the two values *i.e.* either 0 or 1.

Logic Operation

The *OR* gate has an **output of 1 when either A or B or both are 1**.



In other words, it is an **any-or-all** gate because an output occurs when any or all the inputs are present. As seen from Fig. 1 (*b*), the lamp will light up (logic 1) when either switch *A* or *B* or both are closed.

Obviously, the output would be 0 **if and only if both its inputs are 0**. In terms of the switching conditions, it means that lamp would be *OFF* (logic 0) only when both switches *A* and *B* are *OFF*.

The *OR* gate represents the Boolean equation $A + B = X$. The meaning of this equation is that *X* is true when either *A* is true or *B* is true or both are true. Alternatively, it means that output *X* is 1 when either *A* or *B* or both are 1.

OR Gate Symbolizes Logic Addition

According to Boolean algebra, *OR* gate performs **logical addition**. Its truth table can be written as given below:

It must be clearly understood that '+' sign in Boolean algebra **does not stand for the addition** as understood in the ordinary or numerical algebra. In symbolic logic, the '+' sign indicates **OR** operation whose rules are given above. In logic algebra, $A+ B = X$ means that if *A* is true *OR B* is true, then *X* will be true. It does not mean here that sum of A and B equals X.

The other symbols used for '+' sign are *U* and *V*. Hence, the above equation could also be written as *AUB* = *X* or *AV B* = *X*.

$$0 + 0 = 0$$
$$0 + 1 = 1$$
$$1 + 0 = 1$$
$$1 + 1 = 1$$

The meaning of the last three logic additions is that output is 1 when either input *A* or *B* or both are 1. The first addition implies that output is 0 ***only when both inputs are 0.*** The meaning of the '+' sign often becomes clear from the context as shown below:

1 + 1 = 2 — decimal addition

1 + 1 = 10 — binary addition

1 + 1 = 1 — *OR* addition

We can put the above *OR* laws in more general terms

A + 1 = 1

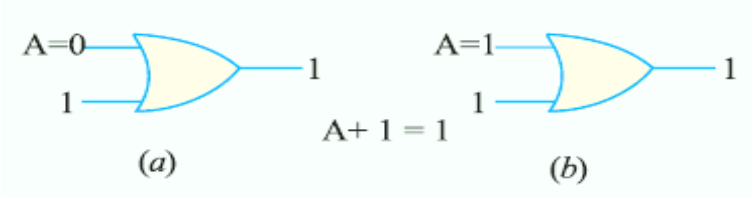
A + 0 = *A*

A + *A* = *A* — not 2 *A*

(*i*) A + 1 = 1

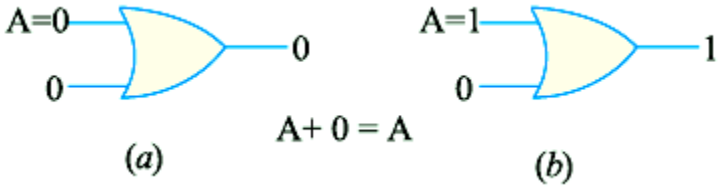
As we know, *A* can have two values: 0 or 1. When *A* is 0, then we have 0 + 1 = 1 as shown in Fig. 2 (*a*). When *A* = 1, then the above expression becomes : 1 + 1 = 1 as shown in Fig. 2 (*b*), Hence, we find that **irrespective of the value of A.**

A + 1 = 1



(*ii*) A + 0 = A

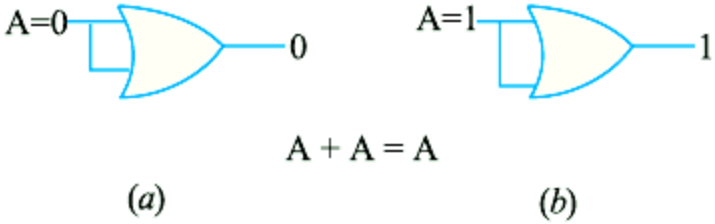
If *A* = 0, then 0 + 0 = 0 *i.e.* output is 0 which is correct and is shown in Fig. 3 (*a*). The output is what the value of *A* is. As shown in Fig. 3 (*b*), when *A* = 1, output is 1 because 1 + 0 = 1. Again, output is what the value of A is.



(*iii*) A + A = A

With *A* set to 0, the output is 0 because 0 + 0 = 0 as shown in Fig. 4 (*a*).

With *A* set to 1, the output is 1 because 1 + 1= 1 as shown in Fig. 4 (*b*). Obviously, the output in both cases is *A*.



<u>The AND Gate</u>

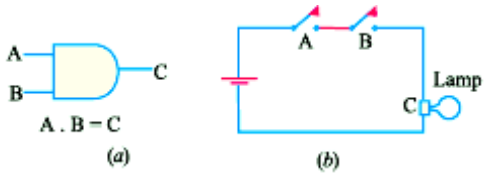
The electronic (or logic) symbol for a 2-input *AND* gate is shown in Fig. 5 (*a*) and its equivalent switching circuit in Fig. 5 (*b*). It is worth reminding the readers once again that the three variables *A*, *B*, *C* can have a **value of either 0 or 1**.

Logic Operation

1. The *AND* gate gives an output only **when all its inputs are present**.

2. The *AND* gate has a 1 output when both *A* **and** *B* are 1. Hence, this gate is an **all-or-nothing** gate whose output occurs only when all its inputs are present.

3. In True/False terminology, the output of an *AND* gate will be **true** only if **all its inputs are true**. Its output would be false if **any *of its inputs is false*.** The *AND* gate works on the Boolean algebra $A \times B = X$ or $A \,.\, B = X$ or $AB = X$



It is a **logical** multiplication and is different from the **arithmetic** multiplication. Often the sign '×' is replaced by a dot which itself is generally omitted as shown above. The logical meaning of the above equation is that

1. output *X* is 1 only when both *A and B* are 1.

2. output *X* is true only when both *A and B* are true.

Table

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

AND Gate Symbolizes Logic Multiplication

According to Boolean algebra, the *AND* gate performs logical multiplication on its inputs as given below:

0.0 = 0

0.1 = 0

1.0 = 0

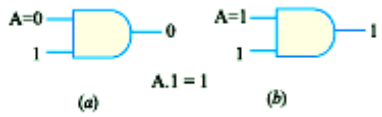
1.1 = 1

In general, we can put the laws of Boolean multiplication in the following form:

$A.1 = A$, $A.0 = 0$, $A.A = A$ — not A^2

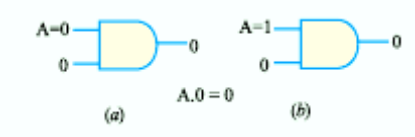
The above indentities can be verified by giving values of 0 and 1 to *A*.

1. A.1 = A When *A* =0 then 0.1 = 0 —Fig. 6 (*a*) When A = 1 then 1.1 = 1 Fig. 6(*b*) It is seen that in each case, output has the same value as that of *A*.



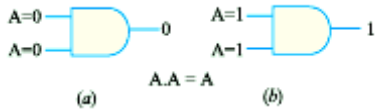
2. A.0 = 0

When *A* = 0 then 0.0 = 0 —Fig. 7 (*a*) When *A* = 1 then 1.0 = 0 — Fig. 7 (*b*). It is seen that output is always 0 ***whatever the value of A*.**



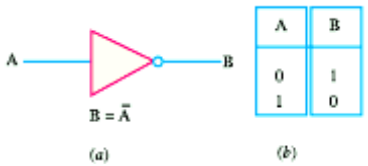
3. A.A = A

When *A* = 0, then 0.0 = 0 — Fig 8(*a*) When *A* = 1, then 1.1 = 1 — Fig. 8 (*b*). It is seen that output always ***takes on the value of A*.**



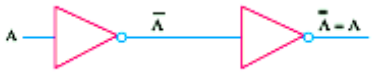
The NOT Gate

It is so called because *its output is NOT the* ***same as its input.*** It is also called an ***inverter*** because it inverts the input signal. It has **one** input and **one** output as shown in Fig. 9 (*a*). All it does is to invert (or complement) the input as seen from its truth table of Fig. 9 (*b*). The schematic symbol for inversion is a small circle as shown in Fig. 9 (*a*). The logical symbol for inversion or negation or complementation is a bar over the function to indicate the opposite state. Sometimes, a prime is also used as *A*′. For example, A means not-A. Similarly, (A + B) means the complement of (*A*+ *B*).



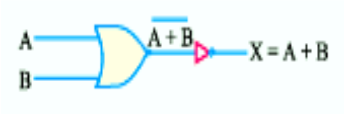
The NOT Operation

It is a ***complementation*** operation and its symbol is an **overbar**. It can be defined as under: As stated earlier, 0 means taking the negation or complement of 0 which is 1. $\overline{0}$= 1. $\overline{1}$=0. It should also be noted that complement of a value can be taken repeatedly. For example, $\overline{\overline{1}} = \overline{0}$ =1 or $\overline{\overline{0}} = \overline{1}$ = 0. As seen double complementation gives the original value as shown in Fig. 10.



The NOR Gate

In fact, it is a *NOT-OR* gate. It can be made out of an *OR* gate by connecting an inverter in its output as shown in Fig. 11 (*a*). The output equation is given by $X = A + B$. A *NOR* function is just the reverse of the *OR* function.



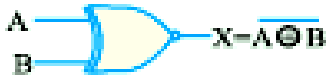
The NAND Gate

It is, in fact, a *NOT-AND* gate. It can be obtained by connecting a NOT gate in the output of an AND gate as shown in Fig. 12. Its output is given by the Boolean equation. This gate gives an output of 1 if its ***both inputs are*** **not 1**. In other words, it gives an output 1 if **either A or B or both are 0**. The truth table for a 2-input *NAND* gate is given in Fig. 12. It is just the opposite of the truth for *AND* gate. It is so because *NAND* gate performs reverse function of an *AND* gate.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

The XNOR Gate

It is known as a not-*XOR* gate *i.e. XOR* gate. Its logic symbol and truth table are shown in Fig. 13. Its logic function and truth table are ***just the reverse of those for XOR gate.*** This gate has an output 1 if **its both inputs are either 0 or 1**. In other words, for getting an output, its both inputs should be ***at the* same** *logic level* of either 0 or 1. Obviously, it produces **no** output if its two inputs are at the **opposite** logic level.



A	B	X
0	0	1
0	1	0
1	0	0
1	1	1